Negative feedback circuit analysis: Ideal gain and G_loop



To analyze this circuit feedback through current variations and voltage steps, we shall first do some assumptions:

- The circuit will behave very slowly, feedback will begin to feed back on the input after a certain time.

In other words, if an emitter (or base) current (or voltage) will be changed, the transistor will wait some time before changing its state given the new parameters. This comes handy when analysing the circuit step by step.

- We consider input related variations (both current and voltage) only. All constant voltage generators will be considered short circuits, all constant current generators will be considered open (see orange marks).

-We don't consider any resistance seen from transistor bases for the moment, but we consider just the 1/gm impedance on the transistor emitter.

We first need to see the circuit at glance and find we need to find the loop.

It is clear that the loop is in the center of the circuit, involving the chain T1,R1->T3->T2,R2.

In this circuit we see that the voltage on R2 feeds back to T1, generating a feedback.

Is this feedback positive or negative? We'll find out in a moment.

Let's get a feeling of the circuit. We have "a sort" of cascode T1, another cascode T2 and lastly we have a degenerated common source T3. Its emitter degeneration resistance is in fact T2 (cascode).

We need to determine whether the loop goes clockwise or anti clockwise. We kind of already answered to this.

Looking at the circuit, we can say "by heart" that current flows through T1's collector, then drives T3 base, thus generating current through R2. Lastly, voltage that appears on R2 feeds back on T1 base.

Therefore, the loop goes anti clockwise. But let's be more specific.

Please note that the following procedure can both be made with currents and voltages. Once we'll manage to get familiar with this thinking, we can do whatever method is preferred.

①/Input current flows *into* the node, feeding R2 and 1/gm. Based on current directions, we can say that a positive voltage step is applied on T1 collector (in blue). This positive step will become handy for later considerations.

②/Except for input_current*(1/beta) that gets lost in T1 base, all the current flowing through T1 will drive T3 Base (we already said that the bias current gen is off, therefore giving infinite resistance there). Considering T3 base resistance and input_current direction, we determine that a positive voltage step is generated on T3 base

If a positive voltage step appears on T3 base, a negative voltage step will appear on its collector(degenerated common source config) and a positive voltage step will appear on its emitter (emitter follower config). Without doing any calculations at all, we're already sure that Vout of this circuit is indeed negative.

(④/A positive voltage step appears onT3 emitter, considering the current that flows into 1/gm T2 cascode, will propagate through the cascode reaching R2 and T1 base.

Using currents, we can say that the current driving T3 base generates a input_current*beta that goes from bottom to top. This current passes through 1/gm (T2) impedance



and enters T1 base and R2. Given current direction, a positive voltage step appears on T1 base. This last step concludes the qualitative loop analysis.

Looking at the drawings we made, we now have a clear view of the working principle.

There's one more step to make, and this is the important effect that creates the feedback loop. We said earlier that in "some" way Vout on T3 collector feeds back to T1 base.

Is there a virtual ground somewhere? Is there something in the circuit that critically changes this circuit behaviour? Look at the circuit and imagine to disconnect T1 base, tie it to real ground and keep R2 and T2 collector connected. Now the loop is broken. What's the difference between this and our feedback circuit? And more importantly, is this a negative feedback? Well, consider again our original circuit. We see that on step 1 and 4 we determined a positive step on T1 emitter and a positive step on T1 base.

We can qualitatively say that for a given positive voltage step at T1 emitter (that makes T1 conduct more and suck more current through its emitter), "after some time" (remember that we're considering a very slow feedback network) a positive step will appear on T1 base, trying to decrease T1 current(because T1 Vbe decreases).

Hypothetically, if V_base = V_emitter, T1 would then shut off.

Following this last equation, if T1 shuts off, then all input_current flows through R1.

This is the key statement that shows the real feedback effect:

"The loop is trying to shut T1 off in order to get input_current flowing in R1. How does it do this? It drives T1 base".

Now that we have an even clearer idea on how this circuit works, we can go back on the other way round of the loop and see how much Vout/I_in is.

Note that we're considering an ideal feedback here, so qualitatively we say that T1 completely shuts off. But, if that was true, T3 would also shut off, as well as T2. So a positive step on R2 would not appear at all.

In reality, an epsilon (very small portion) of input_current will continue to flow through T1 emitter to keep the feedback game going.

Therefore, we can say that:

__/ V_R1 = input_current * R1

__/ T1 V_base = V_emitter -> on R2 appears the same voltage step on R1

__/ I_R2 =(input_current * R1) / R2 and this current (T1 is off, no corrent flows through the base) will all go into T2 collector

__/ Vout = - I_R2 * R3 = [R3* (input_current * R1)] / R2 (Ideally, do not consider current lost through T2 and T3 bases)

__/Transfer function Vout/I_in = - R3 * R1 / R2 -> Ideal gain

If we weren't sure about signs in these equations, we could as well don't consider them at all.

Finding G_loop



What happens next? We need to compute the *real gain* of the circuit, nobody likes living in perfect gains. To do this, we know from the feedback theory that the real transfer function of the circuit can be found using only two gains: G_ideal and G_loop. We already have the first one, we need to find the latter. The real gain would be G_real = G_id / (1 (-1 / G_loop)) with G_loop<0

Finding G_loop isn't always an easy task and requires a lot of exercise. That said, we can use everything we said earlyer in our favor.

There are several (all correct) ways to compute G_loop, some are stupidly complicated, some require working by heart and be smart. We'll se later what being smart means on this circuit.

G_loop is by definition the gain we found reconducing in some way a point of the loop to itself, covering all the loop backwards.

Ideal points to start compute G_loops in discrete circuits are: gates of MOSFETs (using voltages), bases of BJTs (using currents). Voltages for MOSFETS and currents for BJTs are a smart decision that can save a lot of time. We'll see why in this specific circuit.

Disclaimer: the following procedure takes into account that beta parameter of a BJT can go up to 300 (like in this case, beta= 300) so I_emitter = beta * I_base instead of (beta+1) * I_base Moreover, every constant or signal current/voltage generator has to be off. Input_current will be then open.

Without further ado, G_loop is computed as the following:

U/We start from T3 base, injecting an input current.

2/ That injected current will generate an emitter current I_emitter3 = beta * I_injected

(2)/ The emitter current passes through the cascode

(4)/ The same current is divided between R2 and T1 equivalent base resistance.

Note that T1_resistance = beta (1/gm + R1) =(approx) = beta * (R1) because R1 >> 1/gm (1/gm is in the order of 25:100 ohm, while R1 is several kohm)

(b)/ The current that flows into T1 base generates a current that is I_emitter1 = beta * I_base
(c)/ We covered all the loop. Note that in the drawing the and current different from the original one by its sign. That means G_loop is negative, therefore we have negative feedback.



Why is it stupid to start from a voltage and computing G_loop with voltages instead of currents when using BJTs? Let's see the following G_loop (procedure is kind of like the one earlier discussed but this time analyzing voltage gains):



This G_loop has been computed by forcing an input voltage on T3.

We then find that, after simplifying the equation, the seond G_loop is exactly the same we calculated using currents.

This is good news because this means we nailed the computation two times in a row using different methods, or it means that we failed twice.

This second procedure shows how relations between currents, resistors and beta parameters are exactly the same, no matter the method choosen.

In fact, the G_loop of a negative feedback circuit is always the same (given the same approximations).

BJTs are current controlled, so it's intuitive to choose a current to calculate Gloop.

MOSFETs are voltage controlled instead, so it's obvious that we will have less trouble to apply voltages on the MOSFET gate.

If the circuit analyzed contains both MOSFET and BJT transistor, we should then move in a smart way with calculations to get currents on BJTs (so that we can simply multiply by beta) and voltages on MOS.

Hope this helps

Disclaimer: this circuit has been exctracted from professor Marco Sampietro "Elettronica Analogica" lecture notes. Lecture notes are public on the web, but any kind of copyright belongs to him. Explanation in this excercise is provided "AS IS" just to help students to study analog circuits.