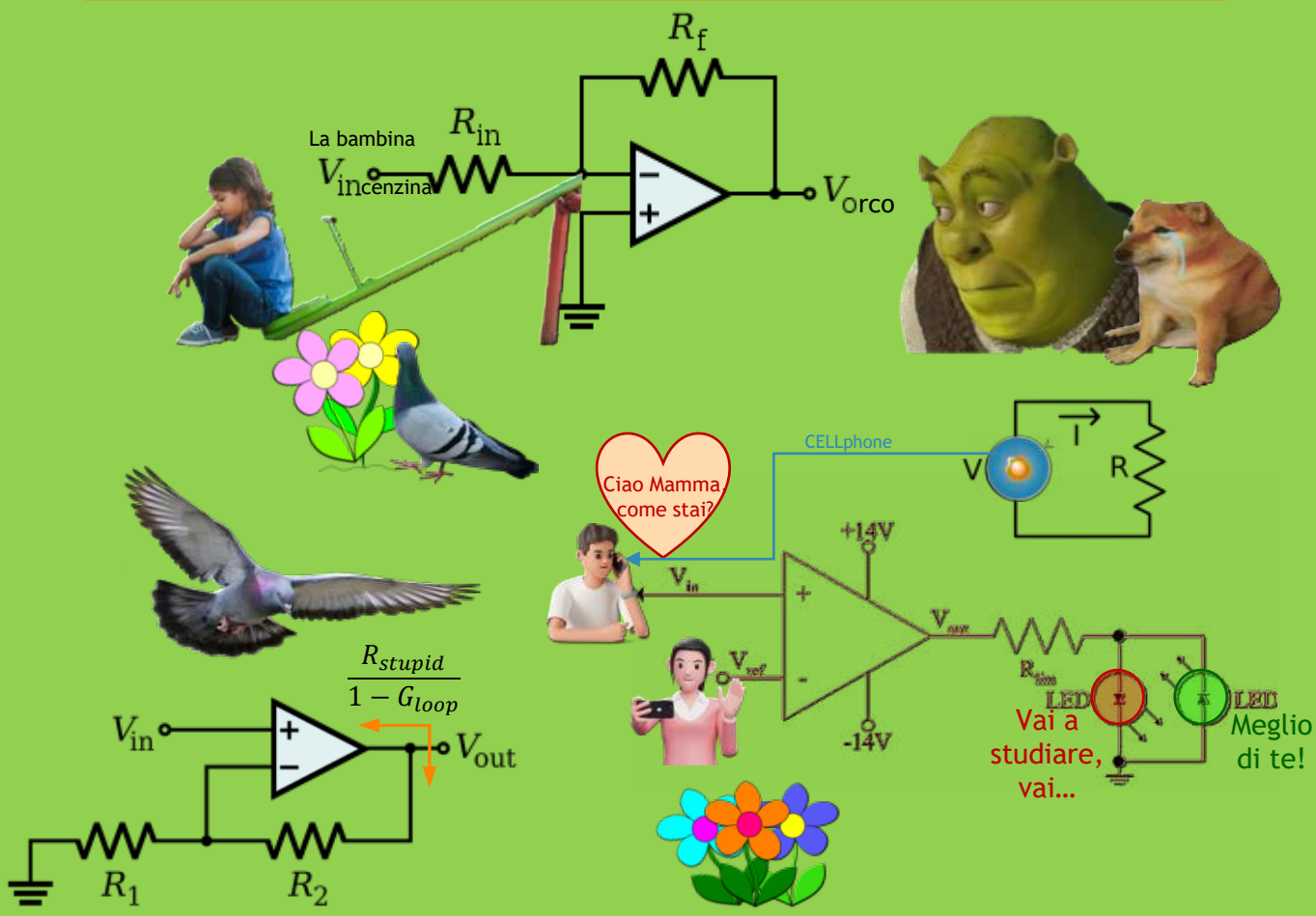
2022/2023



Electronic Systems Summaries

advanced Operational Amplifiers and circuits,
advanced DAC and ADC converters

Franco Zappa

SOCIETÀ EDITRICE CULAPIO

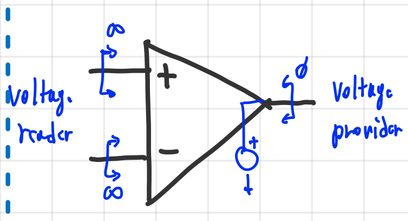
CONTENTS

- OpAmp STAGES
- Different Circuits for Modeling exercises
- DAC
- ADC and advanced ADC

OpAmp types

Summary

VOA

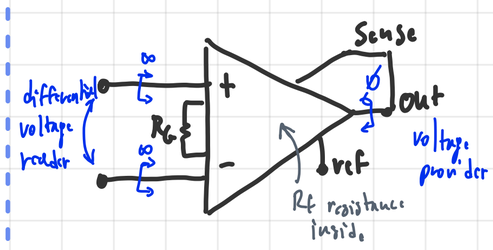


Neg. feed → virtual ground

Pos. feed. → Trigger Smitt

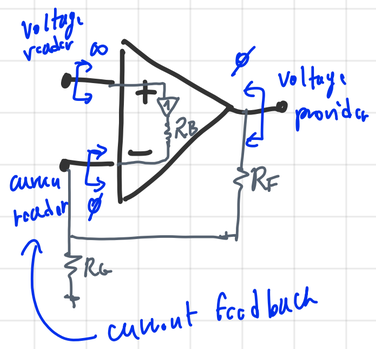
No feed. → Comparator or just amplification till saturation

INA



$$G_{INA} = 1 + \frac{2R_f}{R_G}$$

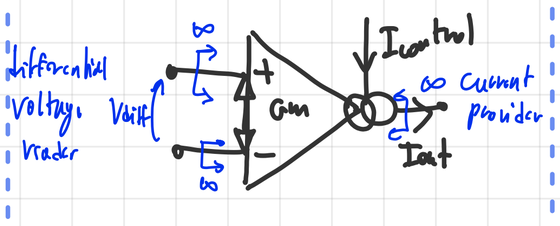
CFA



$$G_{CFA} = 1 + \frac{R_F}{R_G}$$

↖ change this to change the gain

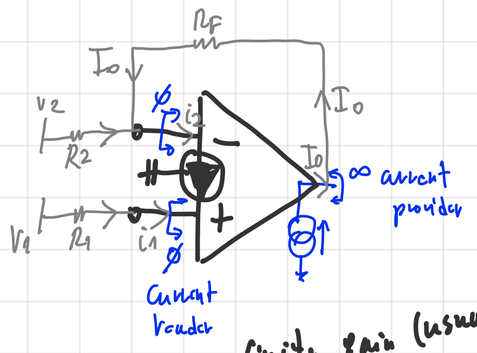
OTA



$$G_{OTA} = \frac{I_{out}}{V_{diff}} = G_m$$

$$G_m = \frac{I_{control}}{\frac{kT}{q}} = \frac{I_{control}}{25mV}$$

NORTON



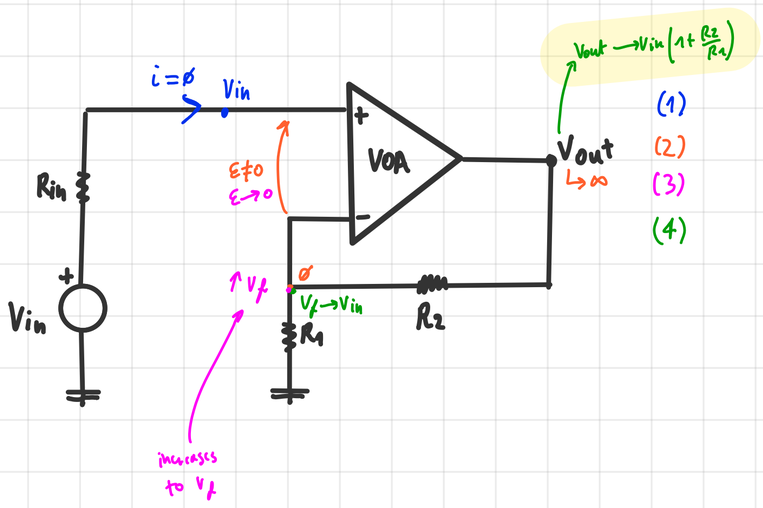
finite gain (usually small)

$$I_{out} = A_i\,(i_1 - i_2)$$

$$V_{out} = \frac{A_i}{1+A_i}\left(V_1\frac{R_f}{R_1} - V_2\frac{R_f}{R_2}\right)$$

VOA

Negative feedback



- $G = 1 + \frac{R_2}{R_1}$
- $\beta = \frac{R_1}{R_1+R_2} = \frac{1}{1+\frac{R_2}{R_1}}$ ($1+\frac{R_2}{R_1} = G$)

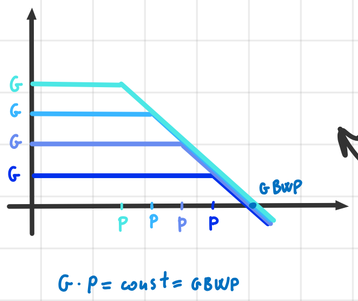
β related to the gain

↳ change the gain (R1 or R2 change)

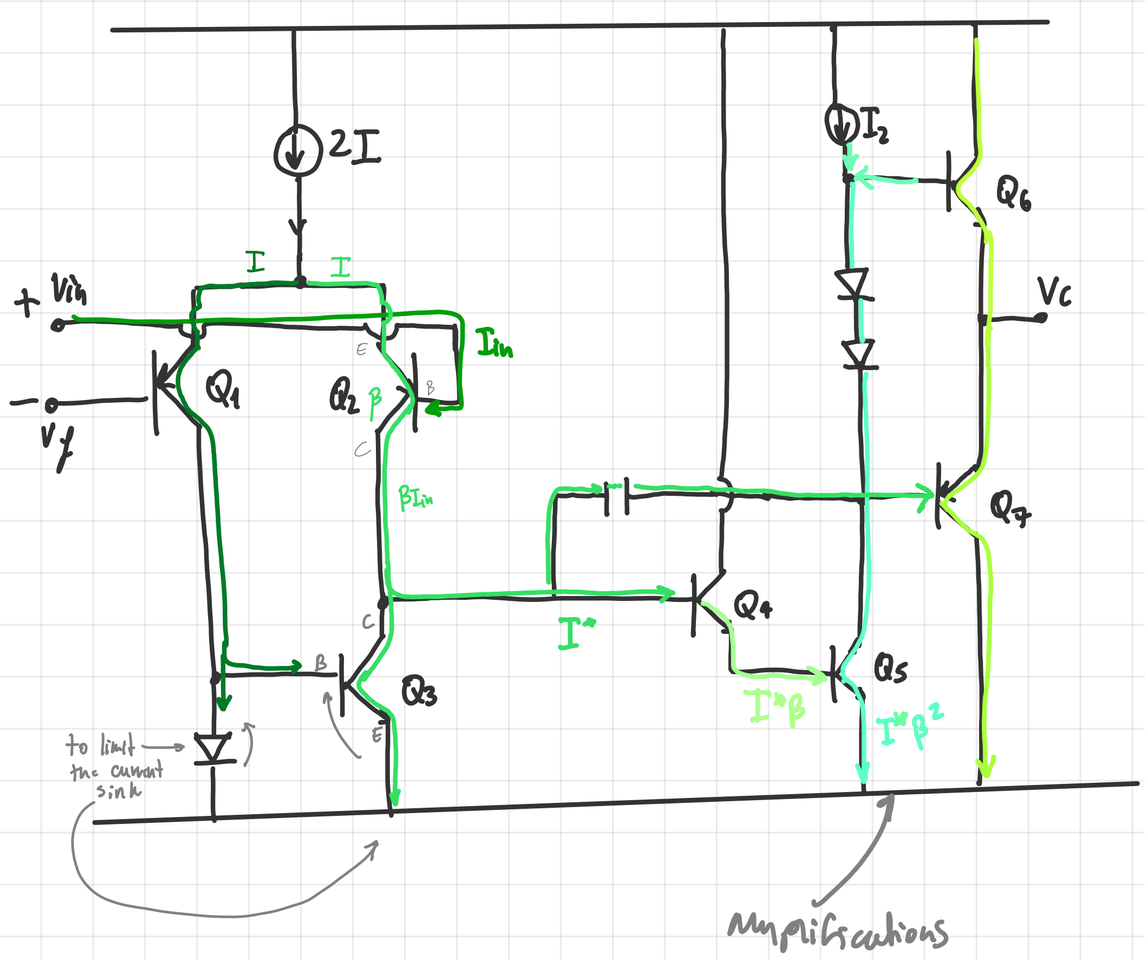
↳ change β

↳ change the pole

GBWP = G·pole = const



Internal Structure



Cons

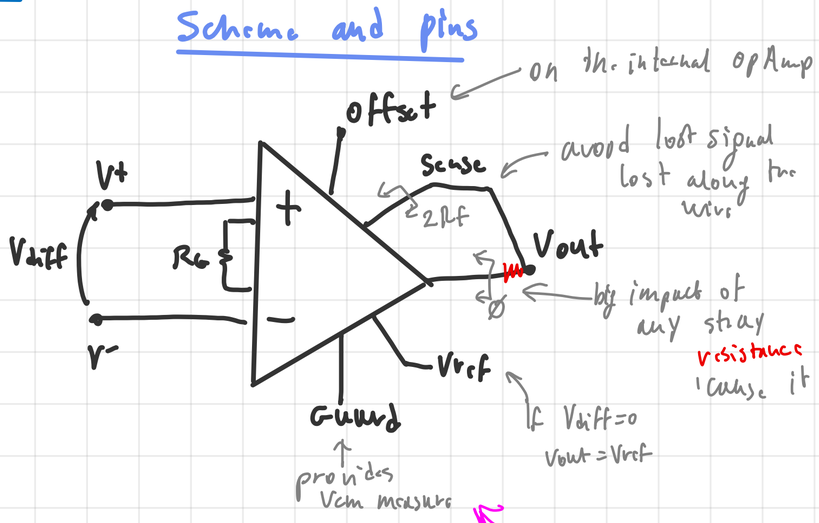
- Cannot have high gain and high BW
- different errors can be improved with other types of OpAmp

Pros

- most common OpAmp
- versatile to build all kind of circuit

INA

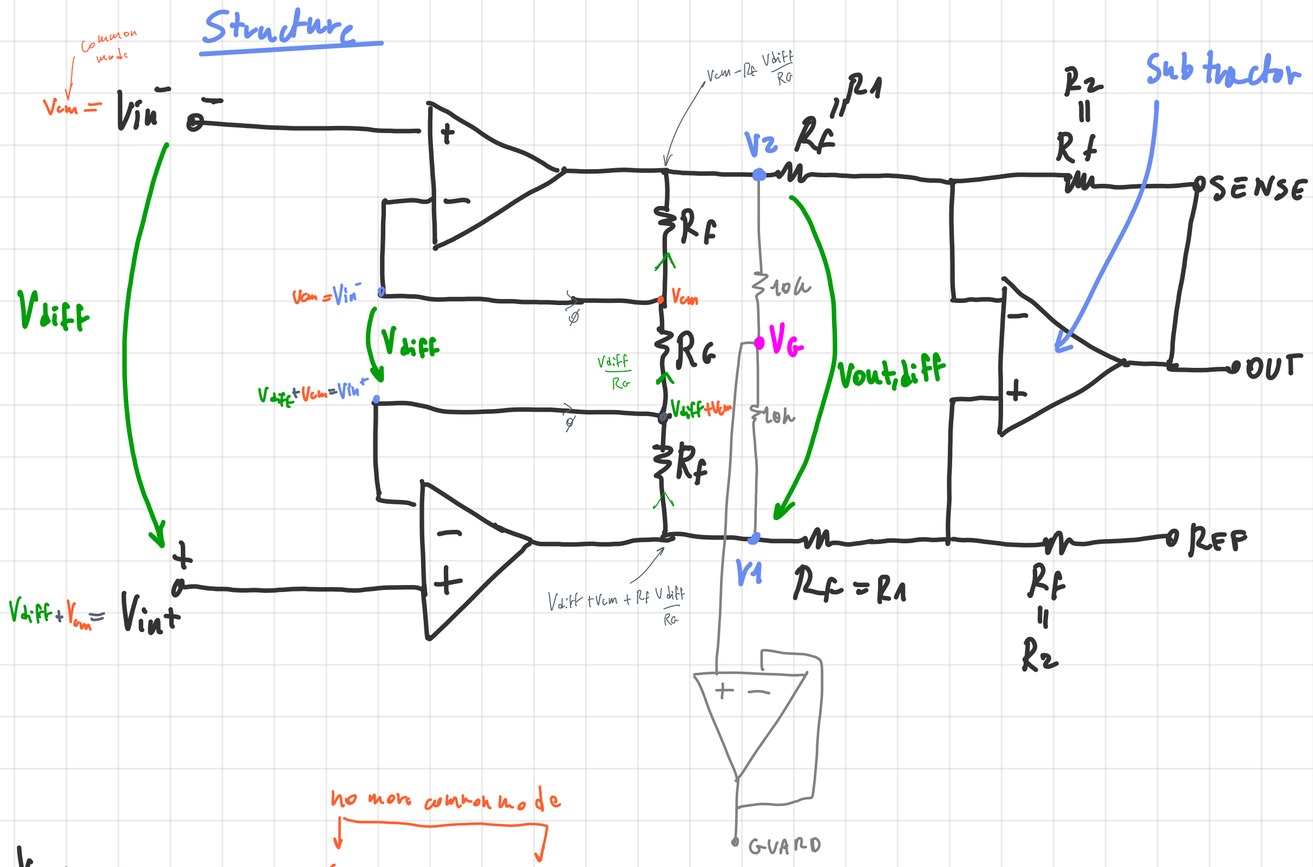
Scheme and pins



$$V_{out} = G_{INA}\cdot V_{diff} + V_{ref}$$

$$G_{INA} = 1 + \frac{2R_f}{R_G}$$

Structure



(*) $V_G = V_{GUARD} = V_1\cdot\frac{10k}{10k+10k} + V_2\frac{10k}{10k+10k} =$

(when Vdiff=0) $\overset{!}{=} \frac{1}{2}\left(V_{diff} + V_{cm} + \frac{R_f V_{diff}}{R_G} + V_{cm} - \frac{R_f V_{diff}}{R_G}\right) = V_{cm}$

no more common mode

↳ $V_{out,diff} = V_{diff} + V_{cm} + R_f\frac{V_{diff}}{R_G} - V_{cm} + R_f\frac{V_{diff}}{R_G} = \left(\frac{V_{diff}}{R_G}\right)\left(R_f + R_G + R_f\right) = V_{diff}\underbrace{\left(1+\frac{2R_f}{R_G}\right)}_{G_{INA}}$

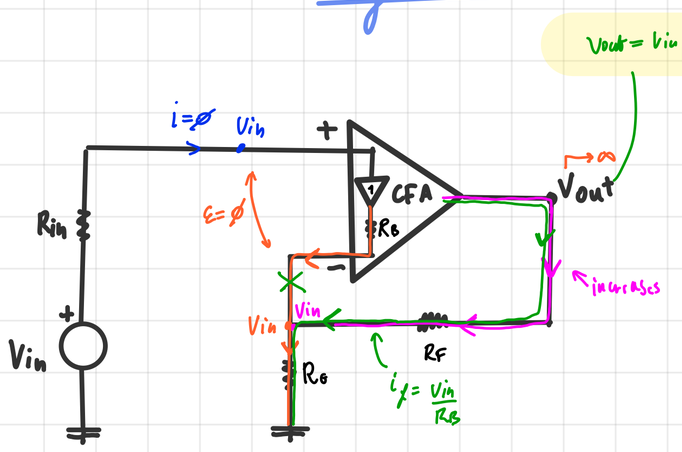
↳ $V_{out} = \underbrace{(V_1 - V_2)\frac{R_2}{R_2}}_{1} + V_{ref} = V_{out,diff} = V_{diff}\cdot G_{INA} + V_{ref}$

Pros:

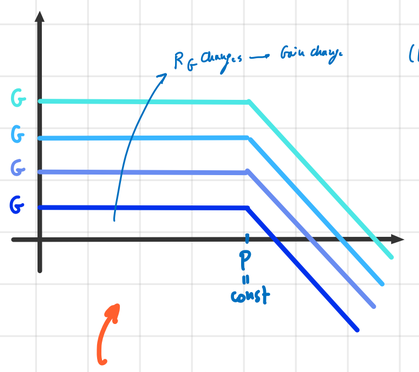
- finite, accurate and reliable Gain
- twin input impedance extremely high (voltage reader)
- extremely low output impedance
- extremely high CMRR (Common Mode Rejection Ratio)

CFA

Negative feedback



- $G = 1 + \frac{R_F}{R_G}$
- $\beta \propto R_F$ ← does NOT depend on R_G
  - ↳ change the gain (by changing R_G)
    - ↳ G_{loop} does NOT change
      - ↳ pole does NOT change

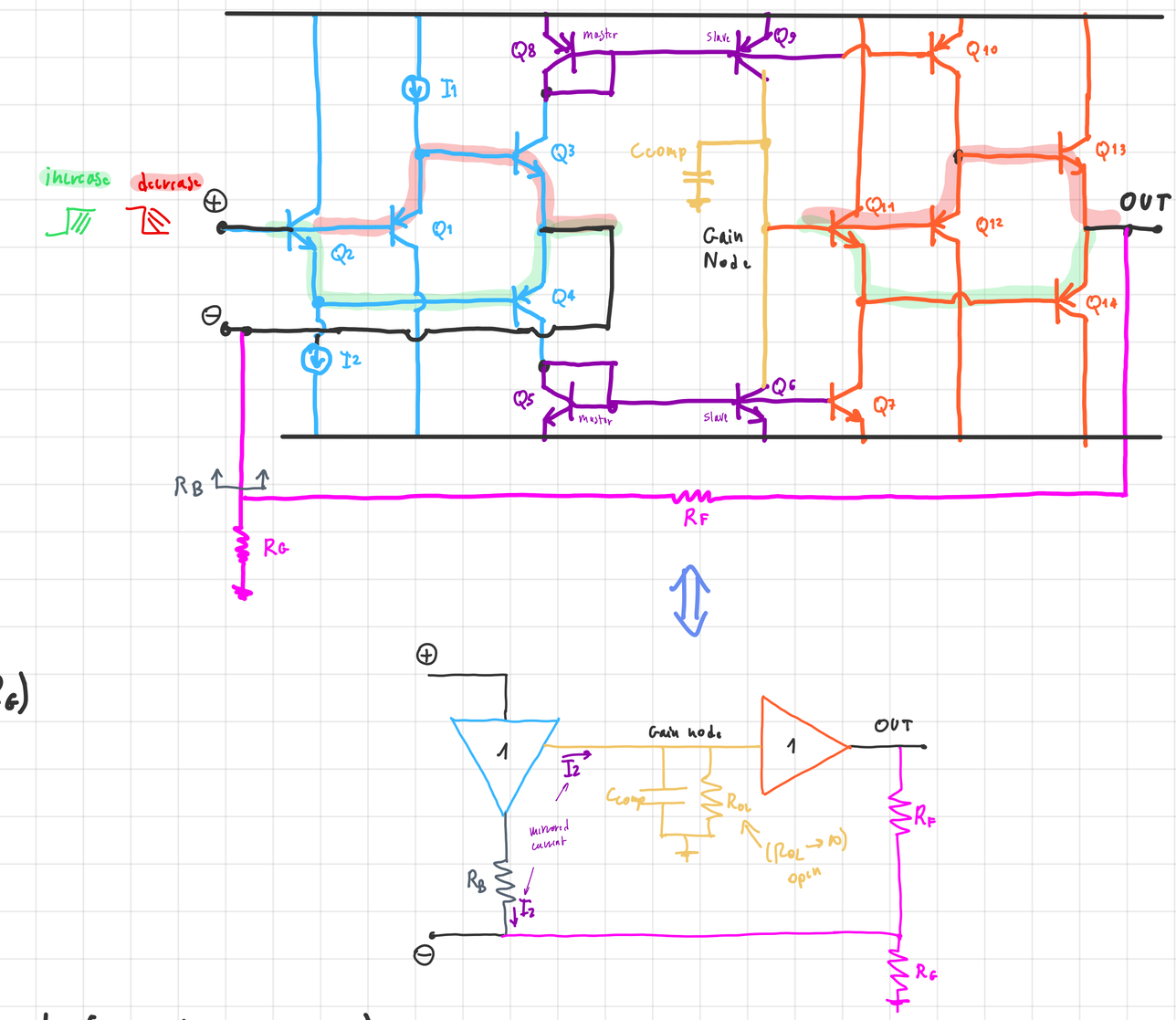


at high gains CFA ≃ VOA
↳ GBWP = const

Pros:
- GBWP ≠ const (for not so high gain)
- Can improve offset and SR (Darling configuration for the buffers)

Cons.
- Has still some errors that have to be compensated using proper circuits (offsets due to temperature, SR limitations due to component slow dynamics, need to use criss-cross config., current mirrors can be improved...)

Internal Architecture



OTA

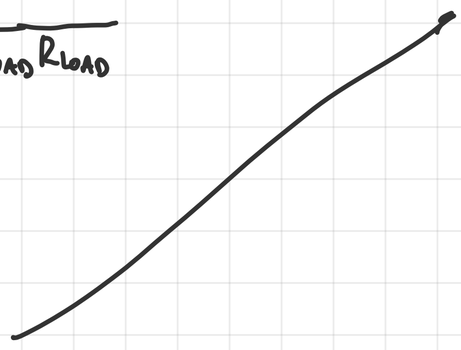
Scheme

this can be used to improve linearity, so putting 2 diodes (from which current can be removed when we want linearization OFF) (higher gain)

$$I_{out} = G_m(I_{control}) \cdot V_{diff} = \frac{I_{control}}{kT/q} \cdot V_{diff} = \frac{I_{control}}{25mV} \cdot V_{diff}$$

Pros:
- all low-impedance nodes
- wide BW → $f_p = \frac{1}{2\pi C_{LOAD} R_{LOAD}}$

Cons:
- no infinite gain
- no virtual ground
- it is used open-loop
- strong nonlinearity

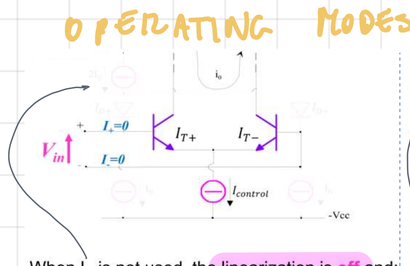


use the TRANSLINGAR PRINCIPLE

$$\prod_{JECW} i_j = \prod_{iECCW} i_i$$

Internal Architecture

OPERATING MODES - LINEARITY

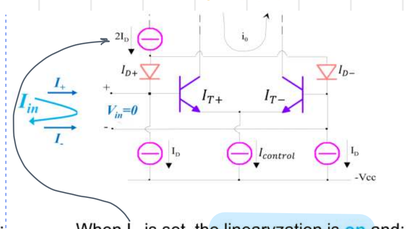


When I_D is not used, the linearization is off and:

$$I_{out} = \frac{I_{control}}{kT/q} \cdot V_{in}$$

when $|V_{in}| < kT/q$

Transconductance amplifier



When I_D is set, the linearyzation is on and:

$$I_{out} = \frac{I_{control}}{I_d} \cdot I_{in}$$

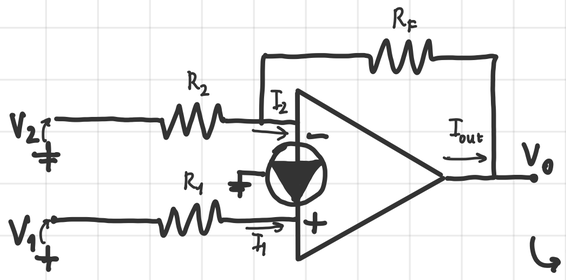
when $|I_{in}| < I_d$

Current amplifier

- case 1: The stage is fully symmetric ($V_{diff} = 0$)
- case 2: ($V_{diff} \neq 0$) $V_{D+} + V_{BE+} = V_{D-} + V_{BE-}$
  - V_{D+} causes I_{c+}
  - V_{D-} causes I_{c-}

NORTON

Negative Feedback



$$I_1 = \frac{V_1}{R_1} \qquad I_2 = \frac{V_2}{R_2} + I_0$$

$$I_0 = \frac{V_0}{R_F} \qquad I_0 = A_i I_{diff}$$

$$I_0 = A_i\left(I_1 - I_2\right) = A_i\left(\frac{V_1}{R_1} - \frac{V_2}{R_2} - I_0\right)$$

$$\hookrightarrow I_0\left(1 + A_i\right) = A_i\left(\frac{V_1}{R_1} - \frac{V_2}{R_2}\right)$$

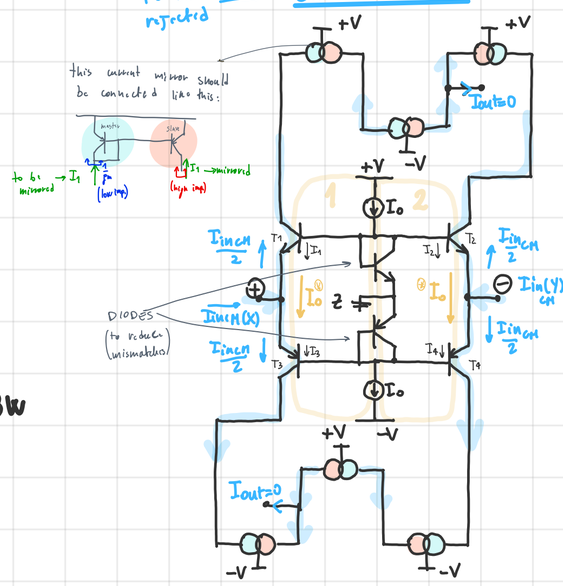
$$\hookrightarrow V_0 = \frac{A_i}{1+A_i}\left(V_1 \frac{R_F}{R_0} - V_2 \frac{R_F}{R_0}\right)$$

Pros:
- It is able to read current inputs
- all nodes have low impedance → parasitic C don't influence the BW
- very high BW (independent from closed-loop gain)

Cons:
- Finite and usually small Ai → No ideal gain behaviour
- Gain depends on external load

Internal Architecture

to be rejected → **Common Mode**

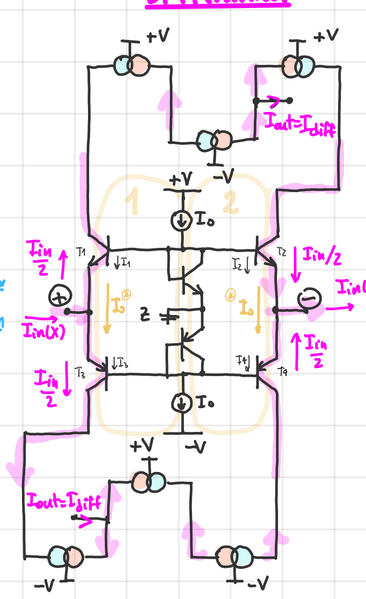


TRANSLINEAR Principle
1 → $I_1 \cdot I_3 = I_0^2$
2 → $I_2 \cdot I_4 = I_0^2$ ⊛

$I_1 = I_2 = I_0 - \frac{I_{incm}}{2}$

$I_3 = I_4 = I_0 + \frac{I_{incm}}{2}$

Differential ← the one we want to amplify



TRANSLINEAR Principle
1 → $I_1 \cdot I_3 = I_0^2$
2 → $I_2 \cdot I_4 = I_0^2$ ⊛

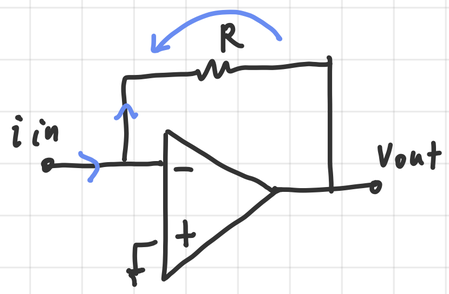
$I_1 = I_4 = I_0 - \frac{I_{in}}{2}$

$I_2 = I_3 = I_0 + \frac{I_{in}}{2}$

MODELING BLOCKS

- ## CONVERTERS

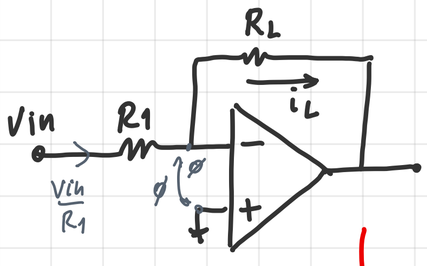
Current - voltage converter



$V_{out} = -R\, i_{in}$

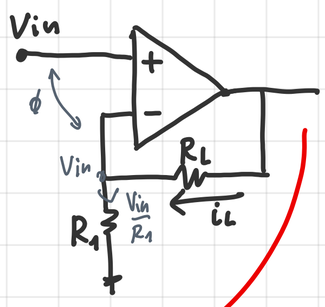
Voltage - current converter

INVERTING



$i_L = \frac{V_{in}}{R_1}$

NON-INVERTING



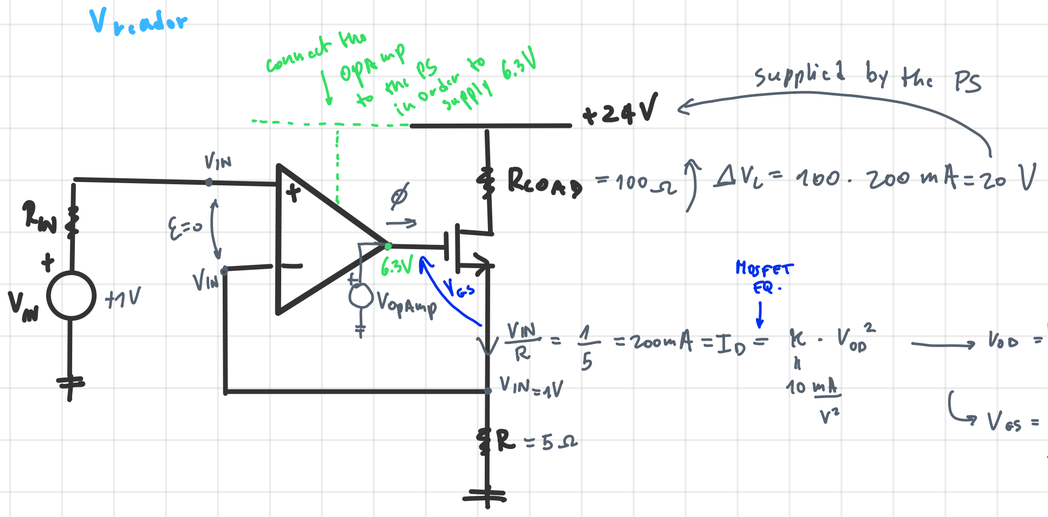
limit on output current

Use this

MOS - transconductance OpAmp

I let the transistor provide the (huge) current needed for the load

Ex.



$\frac{V_{IN}}{R} = \frac{1}{5} = 200\,mA = I_D = K \cdot V_{OD}^2$ (MOSFET EQ.) $\rightarrow V_{OD} = \sqrt{\frac{200\,mA}{10\,\frac{mA}{V^2}}} = \sqrt{20} = 4.2\,V$

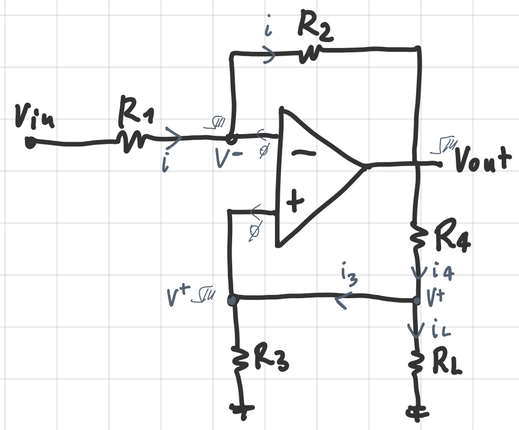
$\hookrightarrow V_{GS} = V_T + V_{OD} = 5.3\,V \Longrightarrow V_{OpAmp} = V_{GS} + V_{IN} = 6.3\,V$ (2)

($V_T = 1.1\,V$)

→ the Op Amp can provide no current but just a voltage, we'll have the current $\frac{V_{IN}}{R}$ floating through the transistor instead of directly the OpAmp

$g_m\big|_{MOS} = \frac{1}{2kV_{OD}}$ on I

Voltage - current converter with load connected to ground



→ $\frac{V_{in} - V^-}{R_1} = i = -\frac{(V_{out} - V^-)}{R_2}$ (1)

$i_4 = i_3 + i_L = \frac{V^+}{R_3} + i_L = \frac{V_{out} - V^+}{R_4}$ (2)

$V^- = V^+$ (negative feedback)

(1) $\frac{V_{out}}{R_2} = \frac{V^-}{R_2} + \frac{V^-}{R_1} - \frac{V_{in}}{R_1}$

$\hookrightarrow V_{out} = R_2\left(\frac{1}{R_1} + \frac{1}{R_2}\right)V^- - \frac{R_2}{R_1}V_{in}$

(2) $i_L = \frac{V_{out}}{R_4} - V^+\left(\frac{1}{R_4} + \frac{1}{R_3}\right)$ (V_{out} ↓)

$i_L = \frac{R_2}{R_4}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)V^- - \frac{R_2}{R_1 R_4}V_{in} - V^+\left(\frac{1}{R_4} + \frac{1}{R_3}\right) =$ (V^- ↓ V^+, $\frac{R_4}{R_3}$)

$i_L = \left[\frac{R_2}{R_4}\left(\frac{R_1+R_2}{R_1 R_2}\right) - \frac{R_4+R_3}{R_4 R_3}\right]V^+ - \frac{R_2}{R_1 R_4}V_{in} = -\frac{R_2}{R_1 R_4}V_{in} = -\frac{V_{in}}{R_3}$

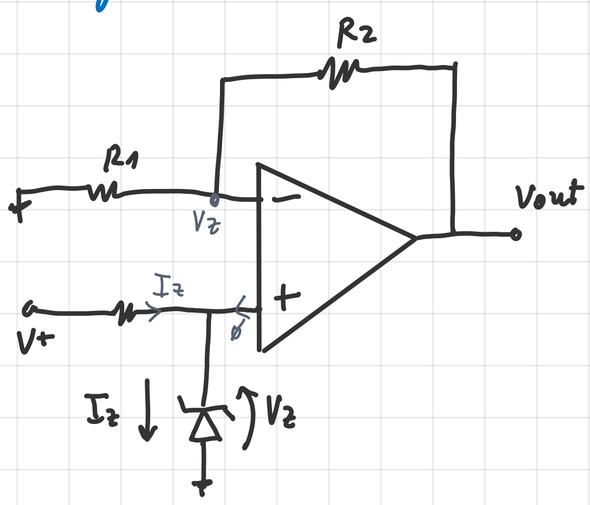
$\frac{(R_1+R_2)R_3 - (R_4+R_3)R_1}{R_4 R_1 R_3} = \frac{R_2 R_3 + R_2 R_3 - R_4 R_1 - R_3 R_1}{R_4 R_1 R_3} = 0$

if we choose $\frac{R_2}{R_1} = \frac{R_4}{R_3}$

$\hookrightarrow R_2 R_3 = R_4 R_1$

$i_L = -\frac{V_{in}}{R_3}$ ←

Voltage reference

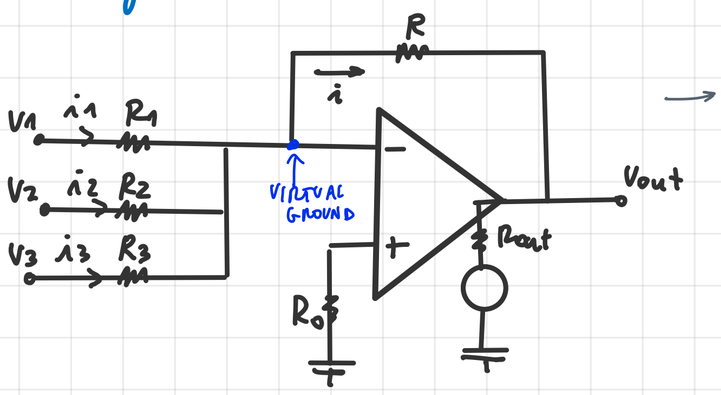


$V_{out} = V_z\left(1 + \frac{R_2}{R_1}\right)$

↳ The input can change the load current I_z without changing the output voltage.

○ OPERATIONAL

Voltage and current adder



→ Computations:

$i_1+i_2+i_3 = i$

$\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}=-\frac{V_0}{R}$

- Voltage GAIN: $V_{out} = -\left(\frac{R}{R_1}V_1+\frac{R}{R_2}V_2+\dots+\frac{R}{R_n}V_n\right) = -R\sum_{i=0}^{n}\frac{V_i}{R_i}$

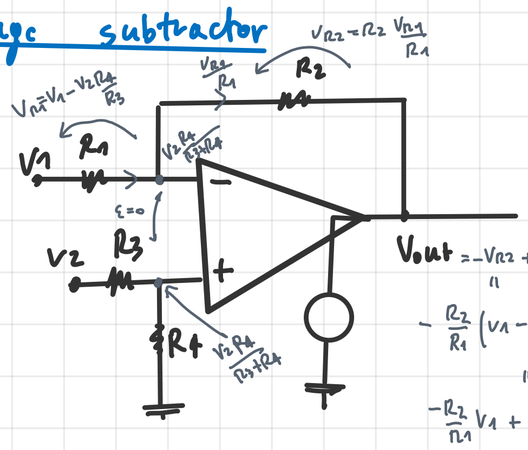
↓ if $R=R_i$

$V_{out} = -(V_1+V_2+\dots+V_n)$

ADDER

- Input Impedance: $Z_{in_i} = R_i$ (for every channel)
- Output Impedance: $Z_{out} \simeq 0$

Voltage subtractor



$V_{out} = -V_{R2}+V_2\frac{R_4}{R_3+R_4}$

$= -\frac{R_2}{R_1}\left(V_1-V_2\frac{R_4}{R_3+R_4}\right)+V_2\frac{R_4}{R_3+R_4}$

$= -\frac{R_2}{R_1}V_1+V_2\frac{R_4}{R_3+R_4}\left(1+\frac{R_2}{R_1}\right) = V_{out1}+V_{out2}$

→ $V_{out_1} = -\frac{R_2}{R_1}V_1$

$V_{out_2} = \frac{R_4}{R_3+R_4}\left(1+\frac{R_2}{R_1}\right)V_2$

$-\frac{R_2}{R_1}V_1+V_2\left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_3+R_4}{R_3}\right) = -\frac{R_2}{R_1}V_1+\frac{R_4}{R_3}V_2$

- Differential GAIN: $\left[\frac{R_2}{R_1}\overset{(*)}{=}\frac{R_4}{R_3}\right]$

$V_{out} = -\frac{R_2}{R_1}V_1+\frac{R_4}{R_3}V_2 = -\frac{R_2}{R_1}(V_1-V_2)$

↓ if $R_1=R_2=R$

$V_{out} = V_2-V_1$

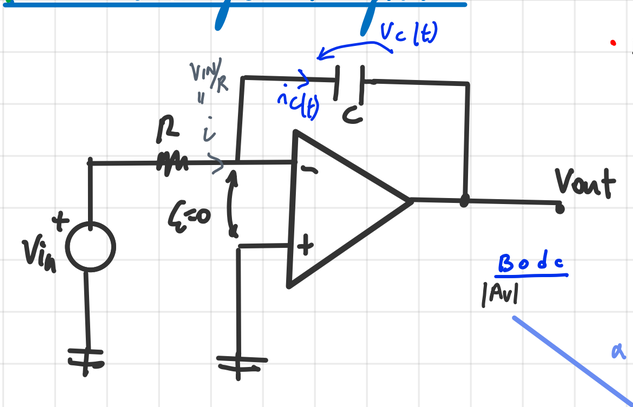
SUBTRACTOR

- Common mode GAIN: $V_{out} = 2\cdot\frac{R_2}{R_1}V_{cm}\cdot tol$
- Input Impedance: $R_{pos} = R_3+R_4$

put buffer at the inputs to solve this → $R_{neg} = R_1$

- Output Impedance: $R_{out} \simeq 0$

IDEAL voltage integrator → Issues → REAL Voltage integrator

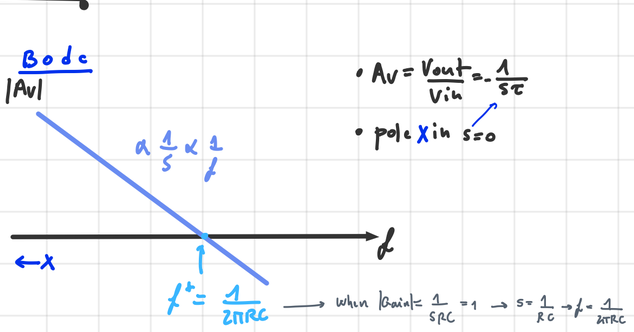


Issues

- DC gain → ∞ (when $f\to 0$ (−∞ in log-log))

⇓

OpAmp will eventually saturate



- $A_V = \frac{V_{out}}{V_{in}} = -\frac{1}{s\tau}$
- pole X in s=0

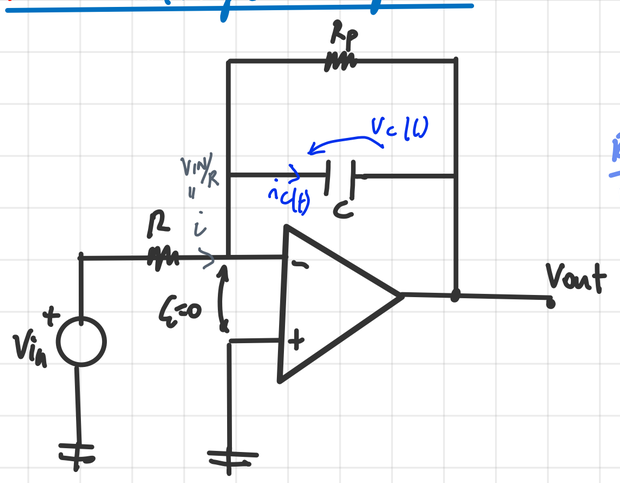
$i(t) = i_C(t) = C\frac{dV_C(t)}{dt}$ ($i(t) = \frac{V_{IN}}{R}$)

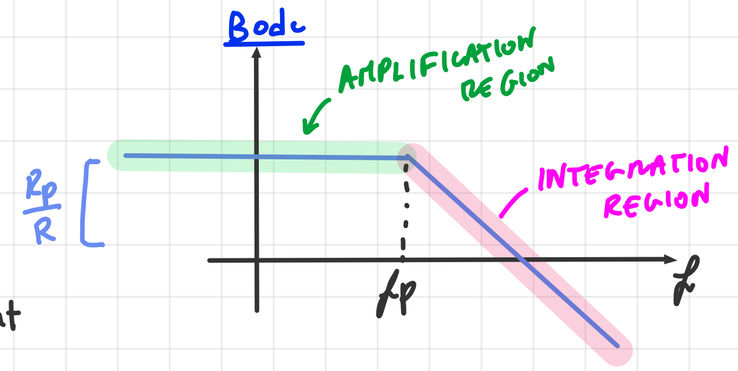
$V_{out} = -V_C(t) = -\frac{1}{C}\int i(t)\,dt = -\frac{1}{RC}\int V_{IN}(t)\,dt$ TIME DOMAIN

↓ LAPLACE TRANSFORM

$V_{out} = -\frac{1}{\frac{RC}{\tau}s}V_{IN} = -\frac{1}{s\tau}V_{IN}$ FREQUENCY DOMAIN

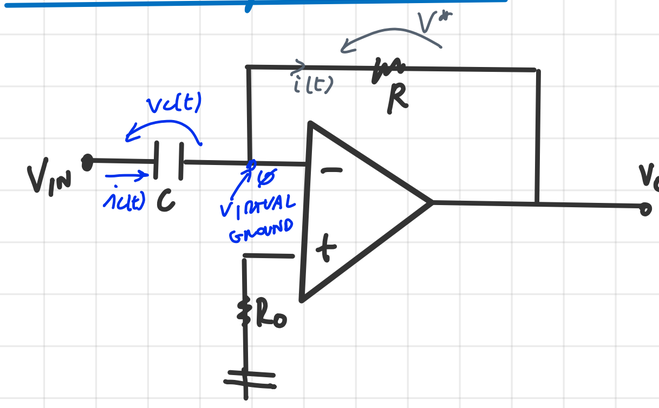
REAL Voltage integrator





- pole at: $f_p = \frac{1}{2\pi R_{eq}C} = \frac{1}{2\pi R_p C}$

IDEAL Voltage Derivator → Issues → REAL Voltage Derivator

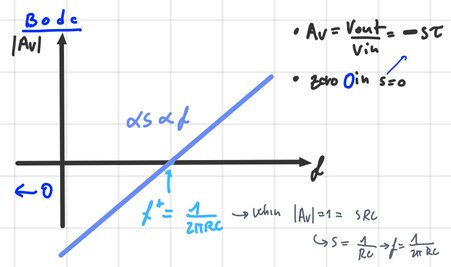


Issues

- HF gain → ∞ (when $f\to\infty$)

⇓

OpAmp will be to sensitive to HF noise



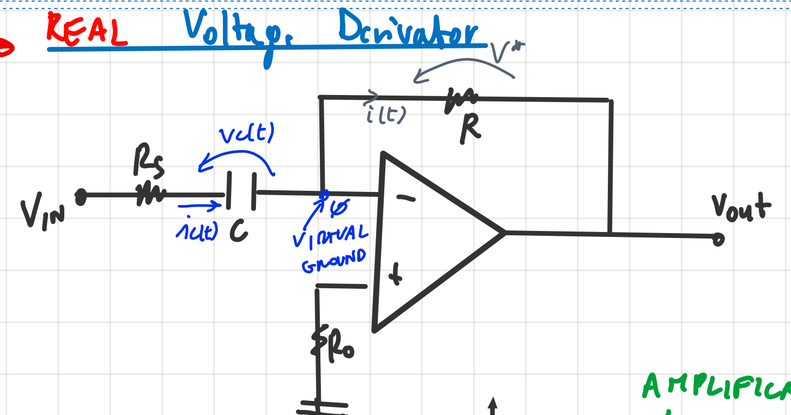
- $A_V = \frac{V_{out}}{V_{in}} = -s\tau$
- zero @ in s=0

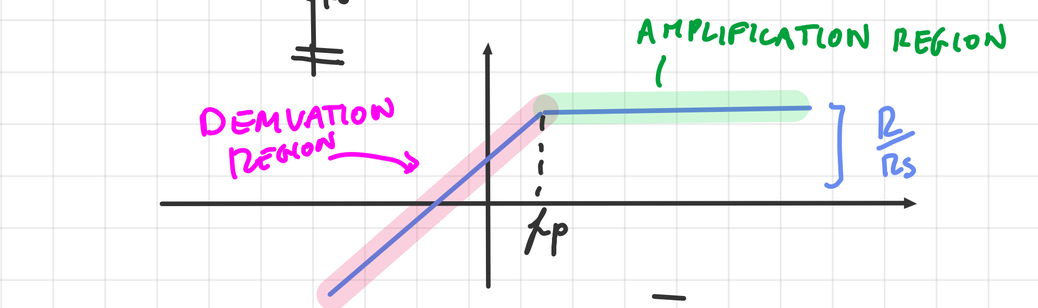
$i(t) = i_C(t) = C\frac{dV_C(t)}{dt} = C\frac{dV_{IN}(t)}{dt}$

$V_{out} = -V^* = -R\,i(t) = -RC\frac{dV_{IN}(t)}{dt}$ TIME DOMAIN

$V_{out}(s) = -\frac{RC}{\tau}s\,V_{IN}(s) = -s\tau\,V_{IN}(s)$ FREQUENCY DOMAIN

REAL Voltage Derivator

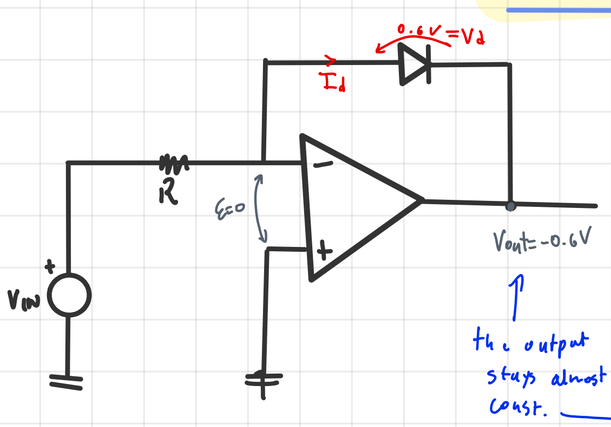


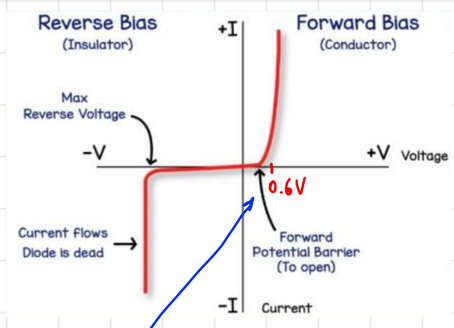


- pole at: $f_p = \frac{1}{2\pi R_{eq}C} = \frac{1}{2\pi R_S C}$

Exponential and Logarithmic CONVERTERS

LOG

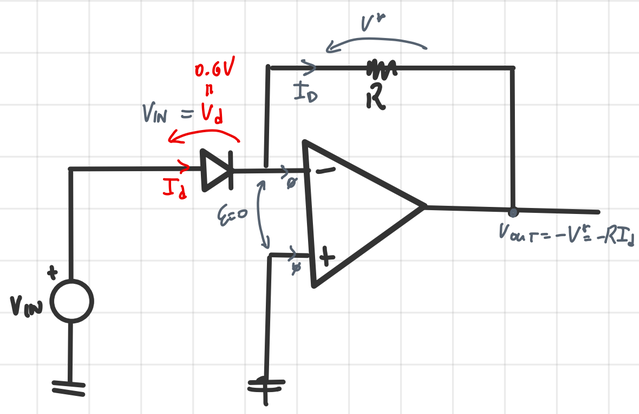


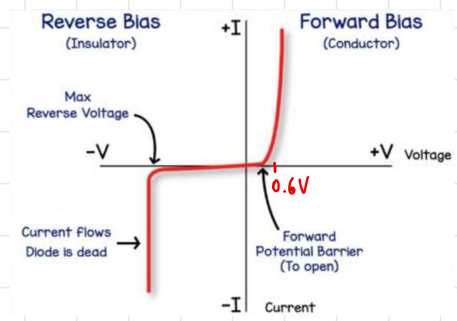


↳ If we analyze the diode equation we know that in the forward region:

- $I_D = I_S\,e^{\frac{V_d q}{kT}}$
- $V_{out} = -V_D = -\underbrace{\frac{kT}{q}}_{V_{TH}}\ln\frac{V_{IN}}{R\cdot I_S} = -V_{TH}\cdot\ln\frac{V_{IN}(t)}{R\cdot I_S}$

EXP

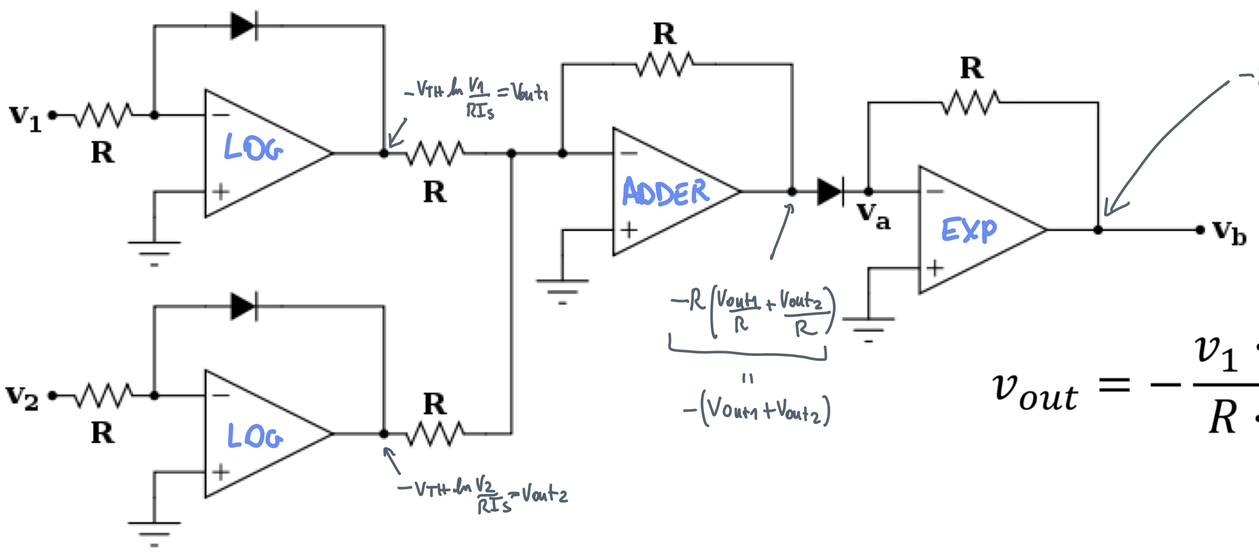




↳ If we analyze the diode equation we know that in the forward region:

- $I_D = I_S\,e^{\frac{V_d q}{kT}}$ ($V_{IN} = V_d$)
- $V_{out} = -V^* = -RI_D = -RI_S\,e^{\frac{V_{IN}q}{kT}}$

Voltage Multiplier



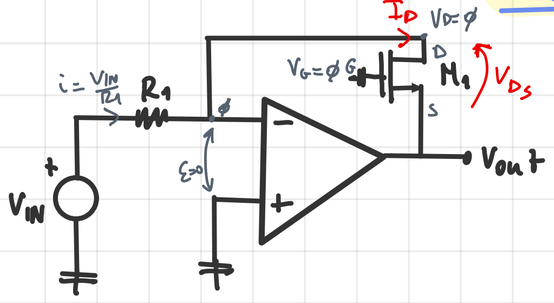
$$-RI_S\, e^{\frac{-(V_{out1}+V_{out2})}{V_{TH}}} = -RI_S\, e^{\frac{+V_{TH}\left(\ln\left(\frac{V_1}{RI_S}\cdot\frac{V_2}{RI_S}\right)\right)}{V_{TH}}} = -RI_S\,\frac{V_1\cdot V_2}{R^2I_S^2} = -\frac{V_1V_2}{RI_S}$$

$$v_{out} = -\frac{v_1\cdot v_2}{R\cdot I_S}$$

We can compute the product between two input voltages!

Square Root And Power 2 Converters

SQRT



MOSFET Equation

to be in the saturated region

threshold $(V_{GS}>V_T)$

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_T)^2 = kV_{OD}^2$$

$\frac{1}{2}\mu C_{ox}$: coefficients; $\frac{W}{L}$: physical property; V_{OD}: overdrive

$$\| \; i \; \| \quad \frac{V_{IN}}{R_1}$$

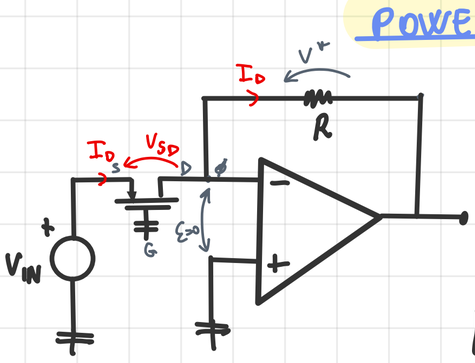
$$V_{OD}^2 = (V_{GS}-V_T)^2 \rightarrow \frac{I_D}{K} = \frac{V_{IN}}{R_1K}$$

$$V_{GS} = V_T + \sqrt{\frac{V_{IN}}{R_1K}}$$

$$V_{OUT} = -V_{DS} = -(V_D-V_S) = V_S = V_G - V_{GS} = -V_T - \sqrt{\frac{V_{IN}}{R_1K}}$$

Square root

POWER2



MOSFET Equation

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_T)^2 = kV_{OD}^2$$

$$V_{out} = -RI_D = -RkV_{OD}^2 = -Rk(V_{IN}-V_T)^2$$

Power 2

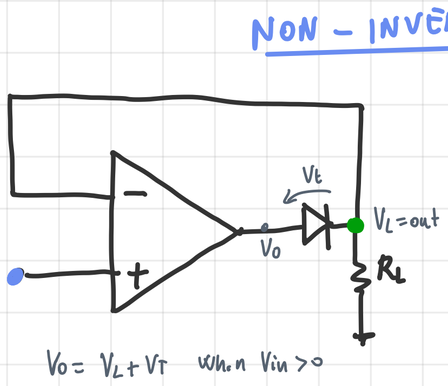
$V_D=0$
$V_S=-V_{IN}$
$V_G=\phi$
$\rightarrow V_{GS}=V_{IN}$

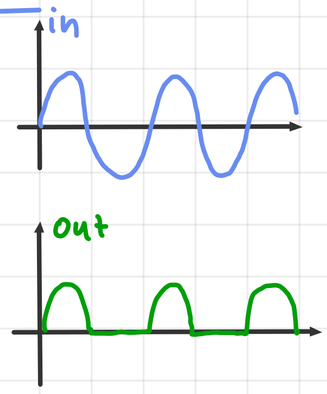
$\rightarrow V_{OD}=V_{GS}-V_T=V_{IN}-V_T$

NON-LINEAR CIRCUITS

Super Diode (Precision Rectifier)

NON-INVERTING

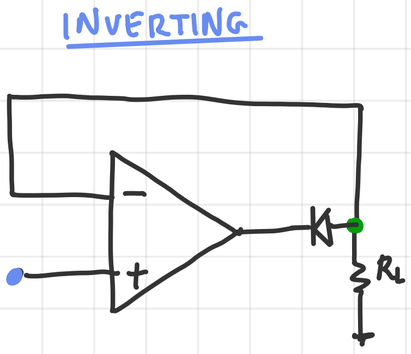


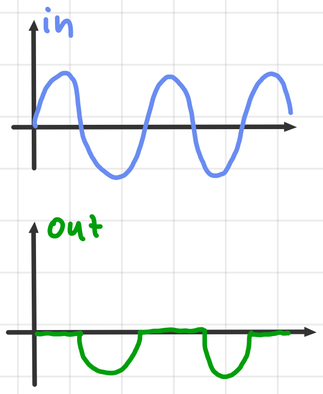


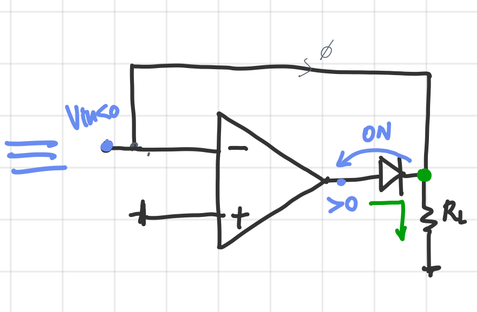
$V_o = V_L + V_T$ when $V_{in}>0$

V_o saturates to $-P.S.$ when $V_{in}<0$

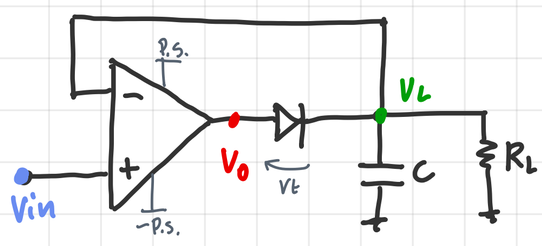
INVERTING

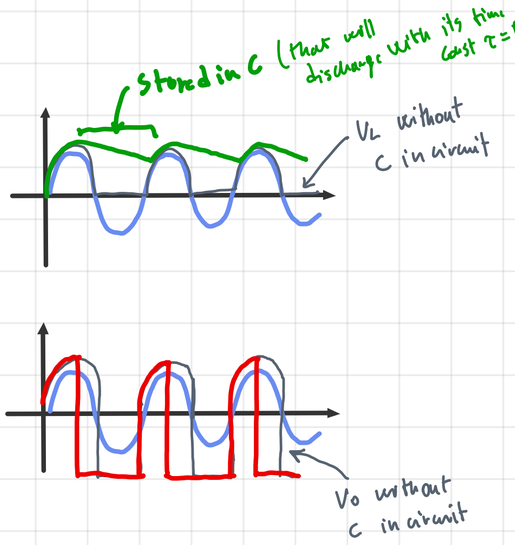






Peak detector

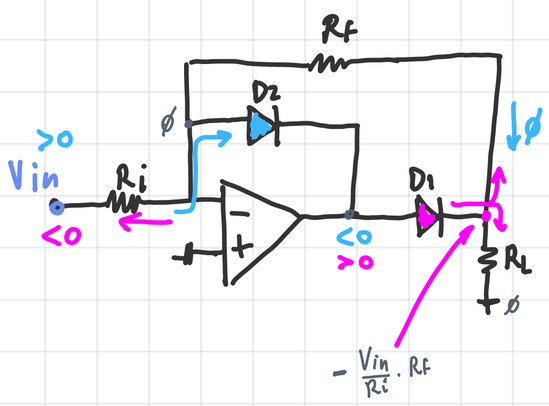


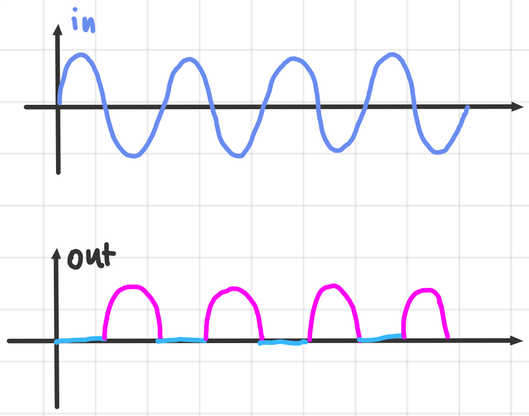


$V_{in}>0$
- $V_o = V_L + V_t$ before reaching the peak $\overline{V_L}$
- when the peak its reached $V_o - \overline{V_L} < V_t$ → diode off (neg. fed from $\overline{V_L}$ $\overline{V_t}$)
- when $V_{in}<0$ → V_o saturates to $-P.S.$

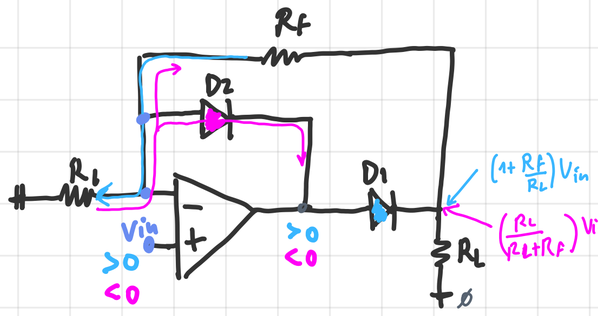
Half-wave rectifier

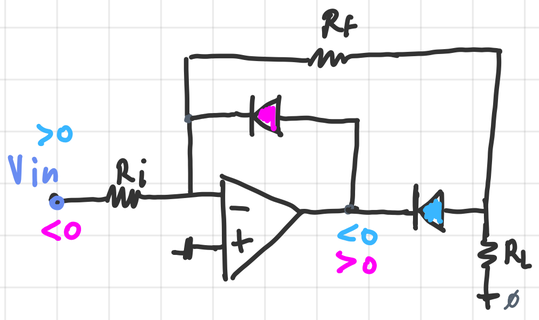
INVERTING



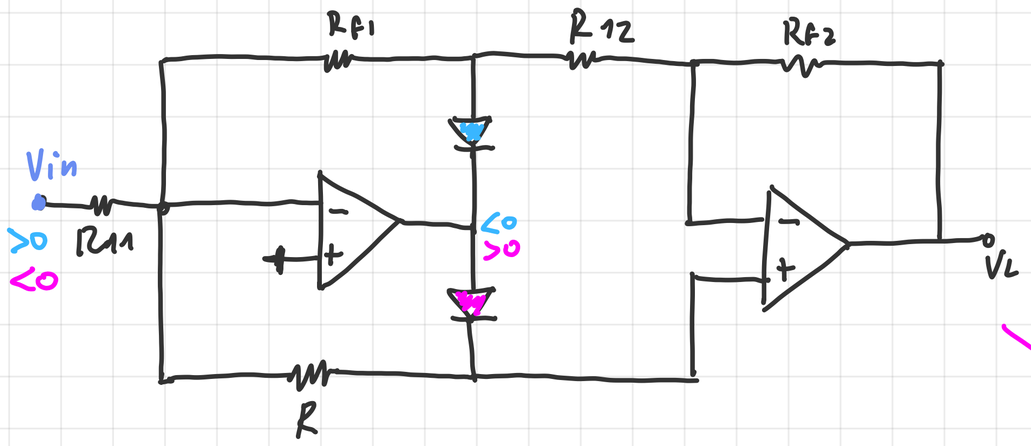


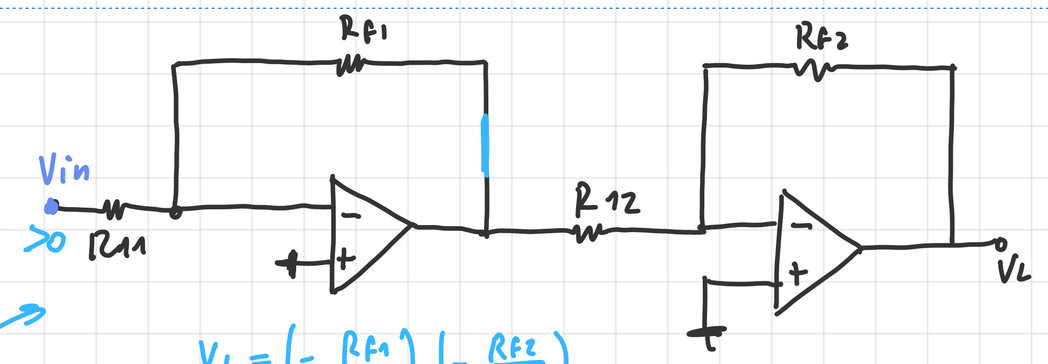
NON-INVERTING



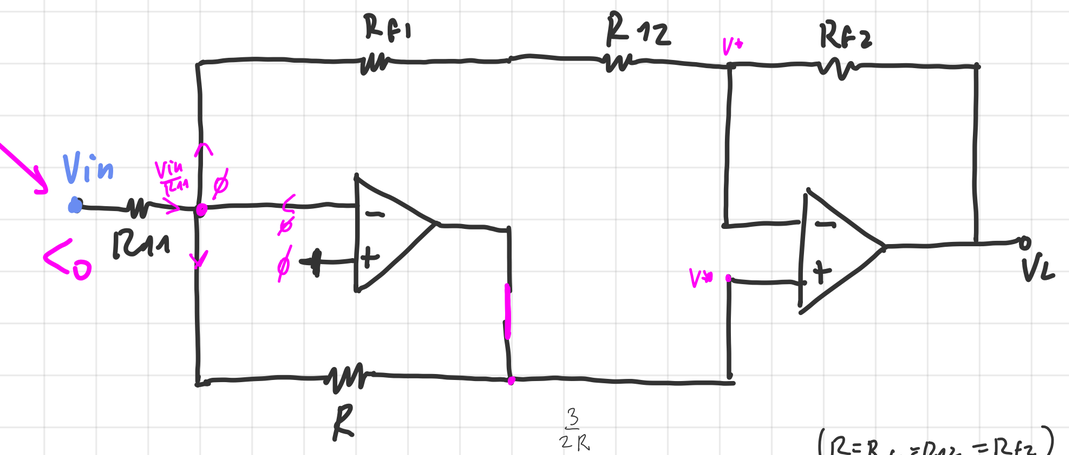


Full-wave rectifier





$$V_L = \left(-\frac{R_{f1}}{R_{11}}\right)\left(-\frac{R_{f2}}{R_{12}}\right)$$



$$-\left(\frac{V^0}{R_{f1}+R_{12}} + \frac{V^+}{R}\right) = \frac{V_{in}}{R_{11}} \longrightarrow V^+\left(\frac{1}{R_{f1}+R_{12}} + \frac{1}{R}\right) = -\frac{V_{in}}{R_{11}} \longrightarrow V^+ = -\frac{2}{3}\frac{R}{R_{11}}V_{in}$$

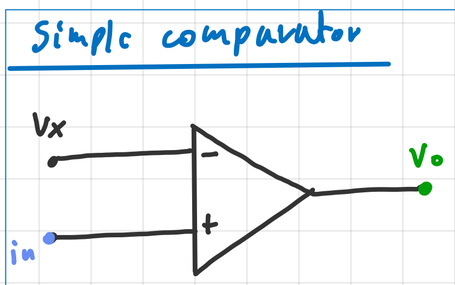
$(R = R_{f1} = R_{12} = R_{f2})$

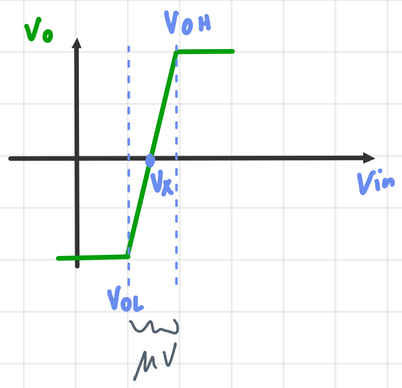
$$V_L = V^+ + \frac{V^+}{2R}\cdot R_{f2} = -\frac{2}{3}\frac{R}{R_{11}}\left(1+\frac{1}{2}\right)V_{in} = -\frac{R}{R_{11}}V_{in}$$

$$V_L = -\frac{R}{R_{11}}V_{in}$$

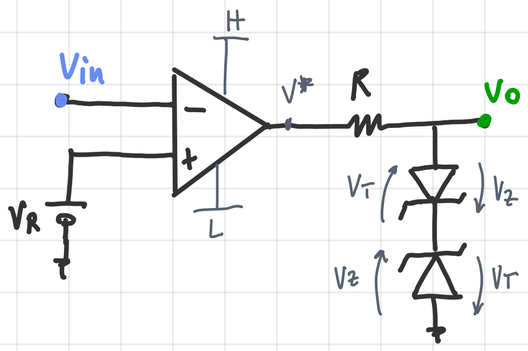
COMPARATORS

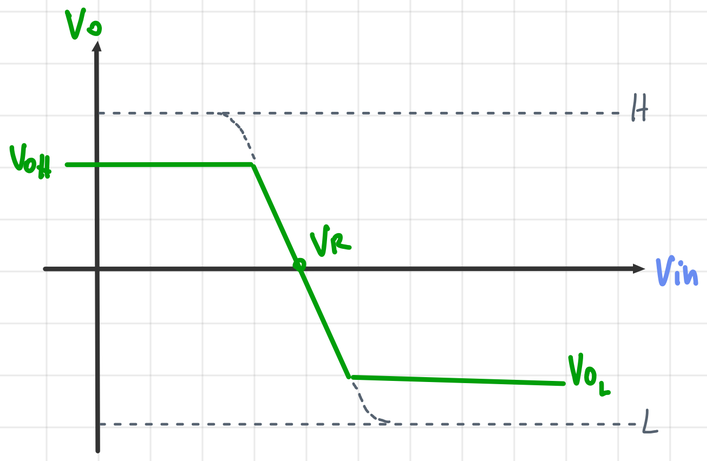
Simple comparator





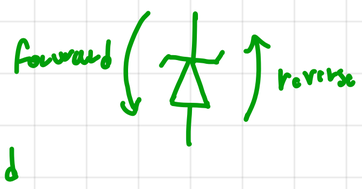
Inverting comparator with zener diodes



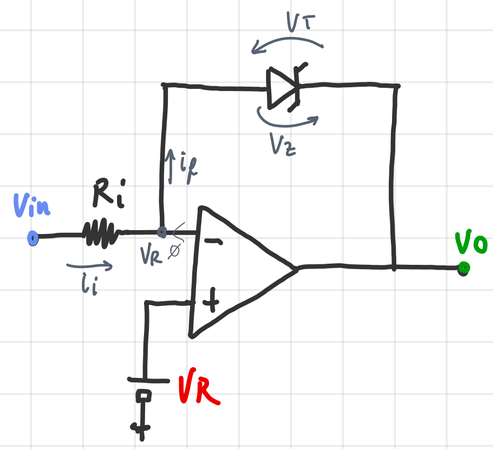


$$V_o = \pm\,(V_z + V_T)$$

reverse, forward

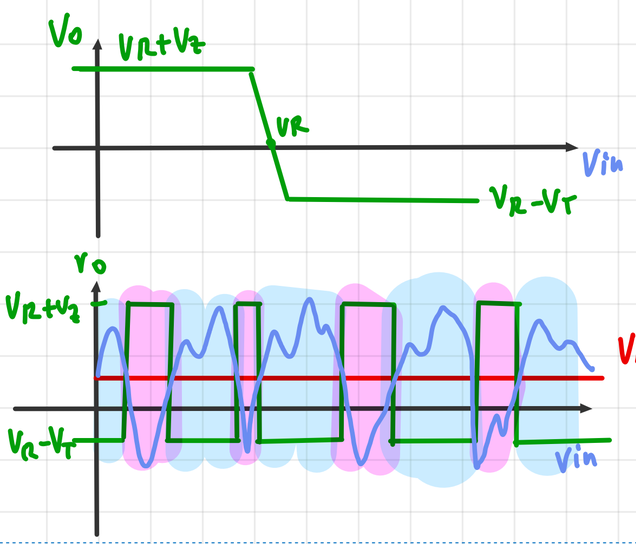


Output voltage limited comparator with feedback zener

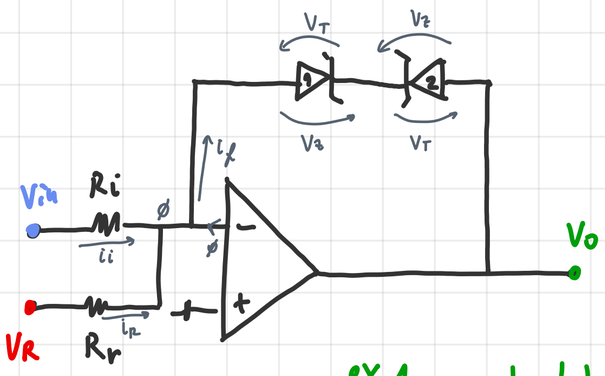


$$i_f = i_i = \frac{V_{in} - V_R}{R_i}$$

- if $V_{in} > V_R$ → forward bias → $V_o = V_R - V_T$
- if $V_{in} < V_R$ → reverse bias → $V_o = V_R + V_z$



Level detector

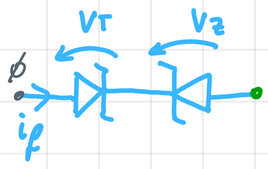


$(R_i = R_r)$

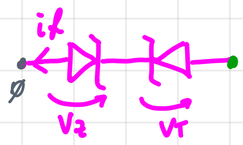
$$i_f = i_i + i_R = \frac{V_{in}}{R_i} + \frac{V_R}{R_r}$$

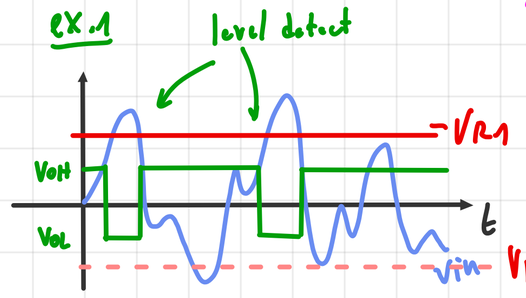
FB = Forward Bias RB = Reverse Bias

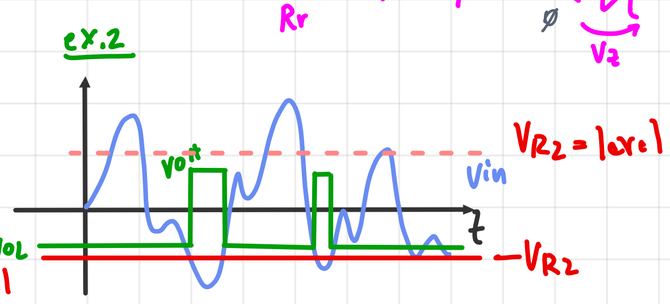
- if $i_f > 0 \rightarrow V_{in} > -V_R\frac{R_i}{R_r} \rightarrow 1 = FB, 2 = RB$ → $V_o = -(V_z + V_T) = V_{oL}$



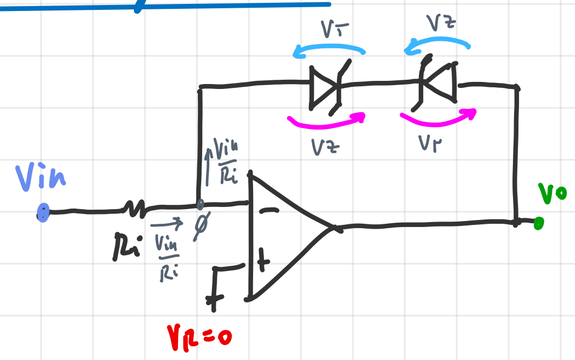
- if $i_f < 0 \rightarrow V_{in} < -V_R\frac{R_i}{R_r} \rightarrow 1 = RB, 2 = FB$ → $V_o = V_z + V_T = V_{oH}$

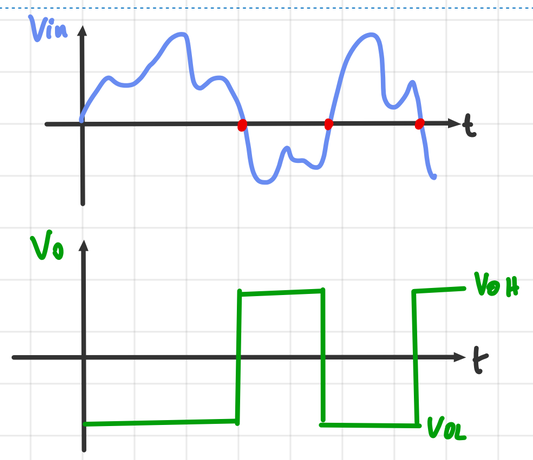






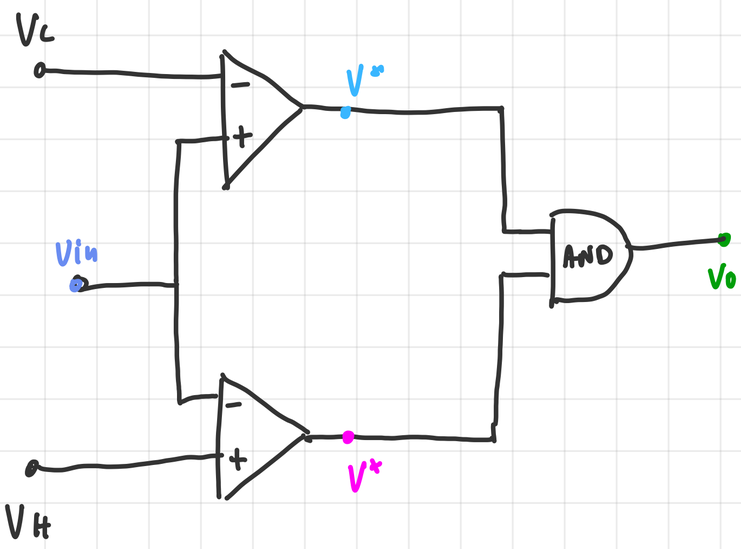
Zero crossing detector

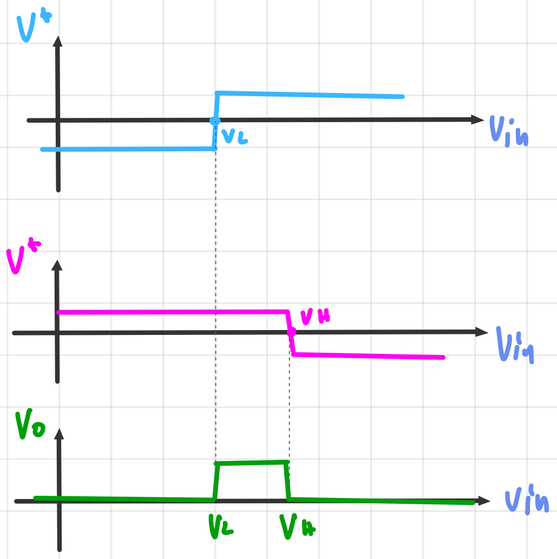




- $V_{oL} = -(V_z + V_r)$
- $V_{oH} = +(V_z + V_r)$

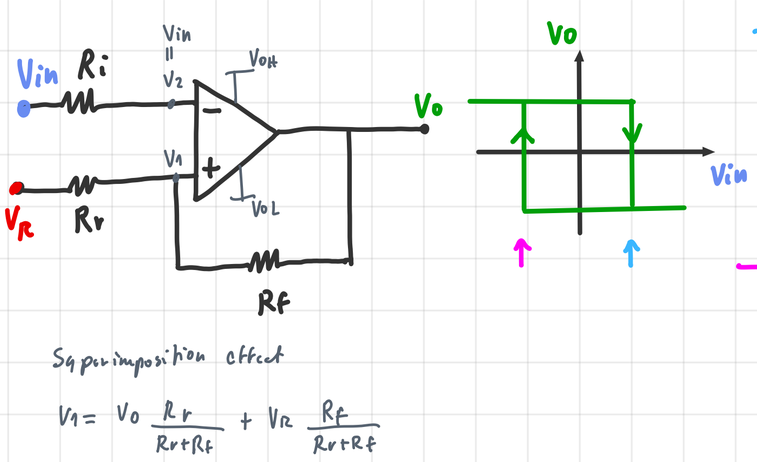
Window comparator





Shmitt trigger

INVERTING



Superimposition effect

$V_1 = V_o \frac{R_r}{R_r+R_f} + V_R \frac{R_f}{R_r+R_f}$

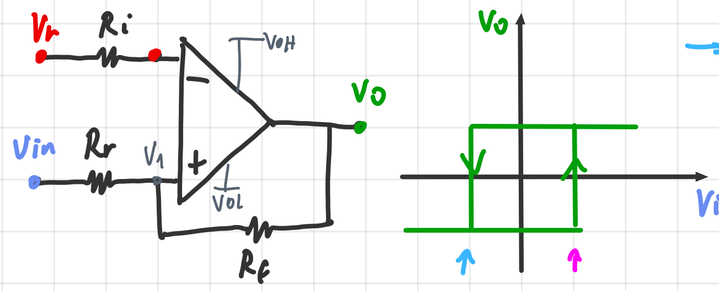
→ If $V_{in} < V_1$ → $V_o = V_{oH}$

$V_1 = V_{TH} = V_{oH} \frac{R_r}{R_r+R_f} + V_R \frac{R_f}{R_r+R_f}$

→ If $V_{in} > V_1$ → $V_o = V_{oL}$

$V_1 = V_{TL} = V_{oL} \frac{R_r}{R_r+R_f} + V_R \frac{R_f}{R_r+R_f}$

NON - INVERTING



$V_1 = V_{in} \frac{R_f}{R_r+R_f} + V_o \frac{R_r}{R_r+R_f}$

↳ $V_{in} = \frac{R_r+R_f}{R_f} V_1 - V_o \frac{R_r}{R_f}$

→ If $V_{in} > V_r$ → $V_o = V_{oH}$

till $V_1 = V_R$ → then switches ↓ $V_{in} = V_{TL}$

↳ $V_{TL} = \frac{R_r+R_f}{R_f} V_1 - \frac{R_r}{R_f} V_{oH}$

→ If $V_{in} < V_r$ → $V_o = V_{oL}$

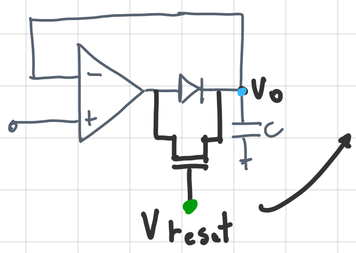
↳ $V_{TH} = \frac{R_r+R_f}{R_f} V_1 - \frac{R_r}{R_f} V_{oL}$

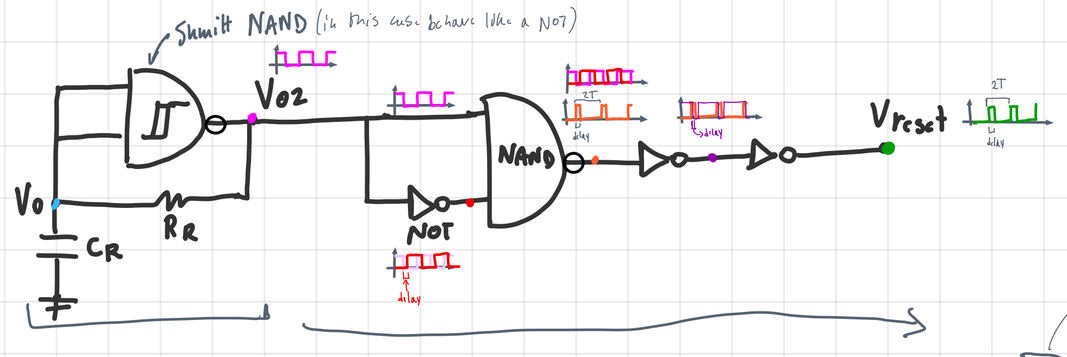
RESET

Reset/Restart circuits

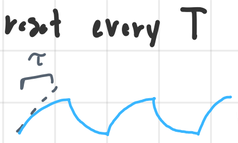
ex. peak detector reset

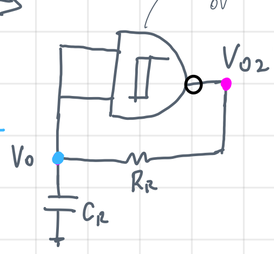
Reset circuit: It's better to wait a little bit to allow the C capacitor to discharge before resetting with $V_{reset} = 0$



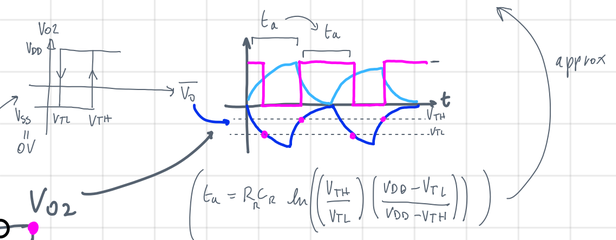


↳ choose $T_{pulse\ reset} \cong \tau = C_R \cdot R_R$ in order to reset every T



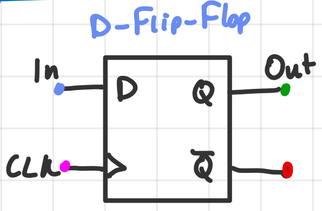


(oscillator)

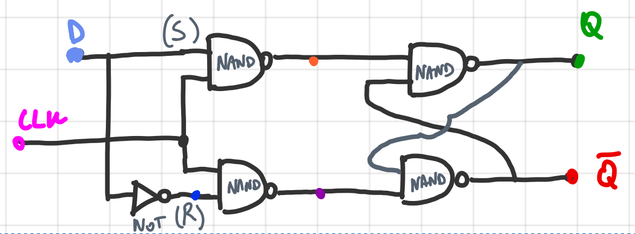


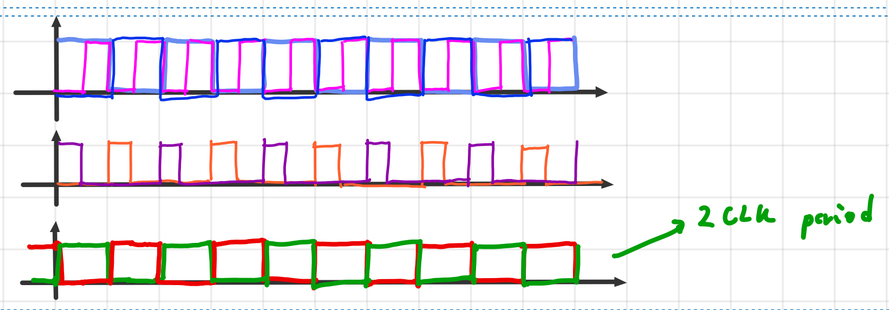
Flip - Flop

D-Flip-Flop

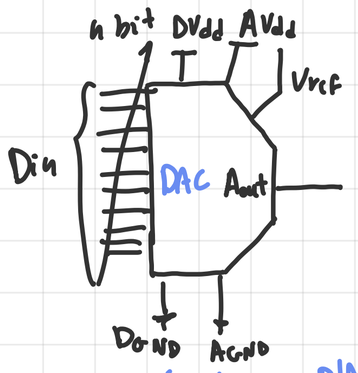


≡





DAC SUMMARY

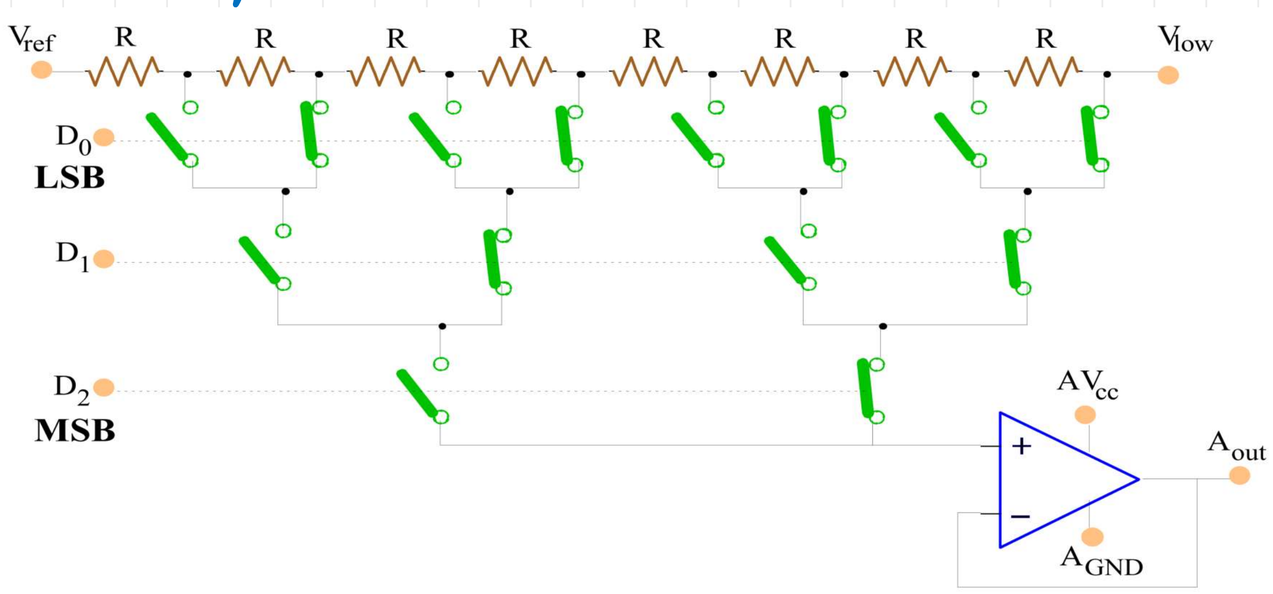


Formula: $A_{out} = \frac{D_{in}}{2^n} V_{ref}$

Separate D/A → avoid A⇆D induced disturbance

P.S.

Voltage-scaling DAC

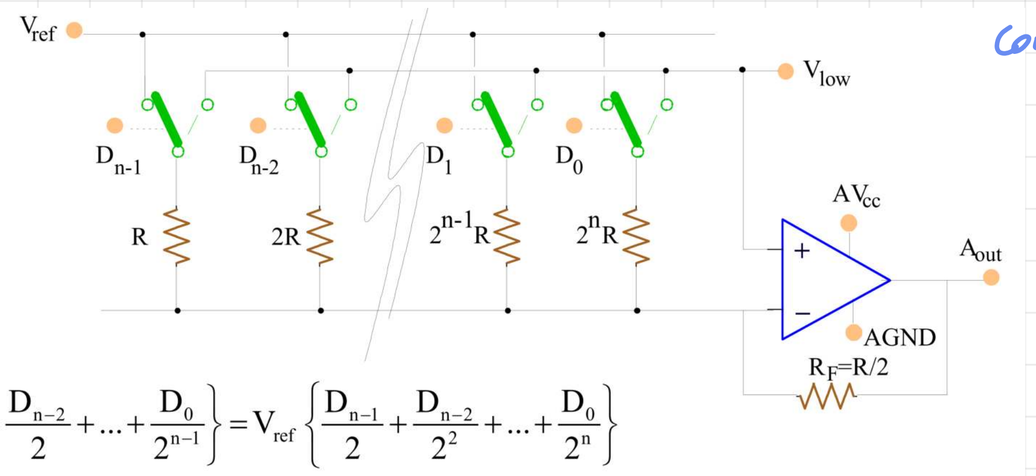


Components:
- 2^n Resistors → divide FSR in 2^n voltage level
- 2^{n+2} MOS → allow to properly select the levels
- Op Amp

Pros:
- MOS switching efficient and less expensive that A. MUX
- easy scalability of all resistors

Cons:
- large # resistors and transistors → too much space
- I_B and I_{leak} cause non-lin.
  - I_B ↓ OA
  - I_{leak} ↓ MOS

Weighted-R DAC



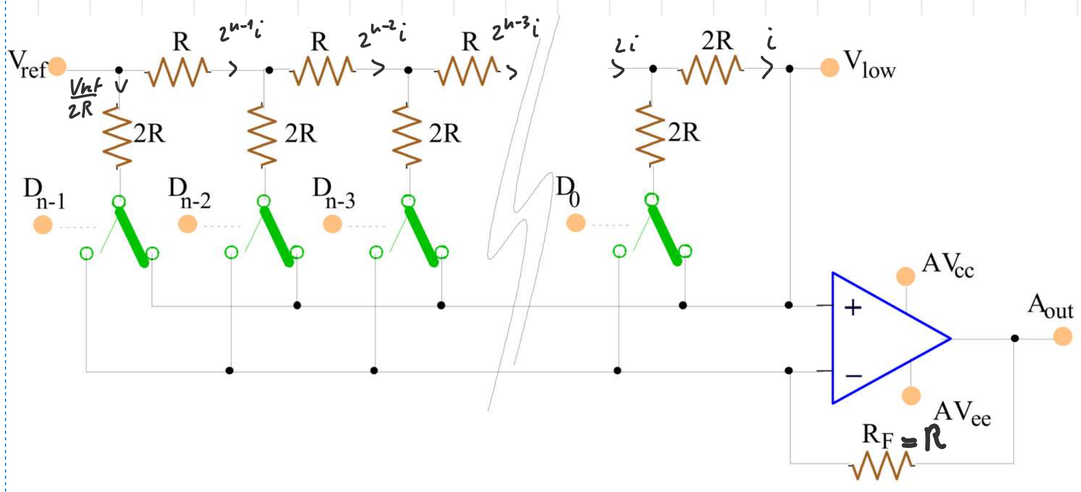
$$V_{out} = V_{ref}\frac{R_f}{R}\left\{\frac{D_{n-1}}{1}+\frac{D_{n-2}}{2}+\ldots+\frac{D_0}{2^{n-1}}\right\} = V_{ref}\left\{\frac{D_{n-1}}{2}+\frac{D_{n-2}}{2^2}+\ldots+\frac{D_0}{2^n}\right\}$$

Components:
- >n resistors → voltage levels
- 2n p/n-MOS
- Op Amp

Pros:
- simplest converter

Cons:
- different R values + tollerances
- voltage drop on R_{ON}, R_S
- variable current consumption
- large silicon area
- I_{bias} errors

Current switching DAC

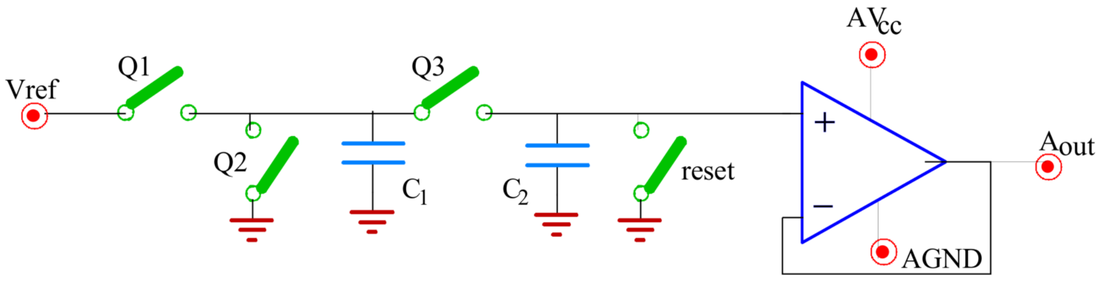


Components:
- 3n resistors → current divider
- 2n MOS → switches low levels
- Op Amp

Pros:
- easy scalability of resistors
- easy drive of MOS switches → R_{ON} creates a const. offset (can be compensated)

Cons:
- bias currents errors

Serial input DAC

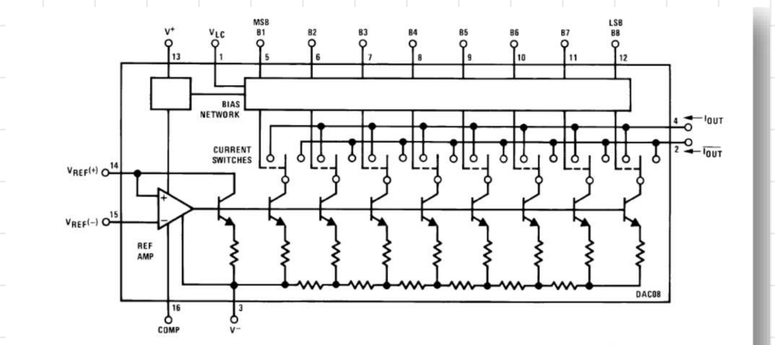


Components:
- only 2 capacitors → C_1 For store and C_2 sharing the bit value
- 5 MOS → close/open to activate store/share logics

Pros:
- Extremely compact and easy

Cons:
- individual bits are provided sequentially (serially) → SLOW

Multiplying DAC



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

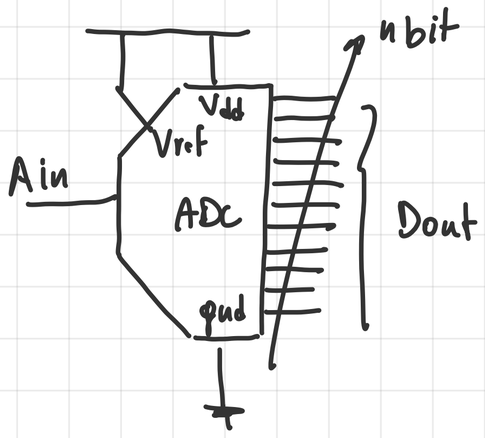
Components:
- ~2n resistors
- ~n mirrors + n switches (current steerer) → to provide $\bar{I}_{out}$, I_{out}
- OpAmp → to vary Vref

$$I_{out} = \frac{V_{ref}}{R_{ref}} \cdot \frac{D_{in}}{2^n}$$ (MULTIPLYING; R_{ref} variable, 2^n variable)

$$I_{out} + \bar{I}_{out} = I_{FS} = \frac{V_{ref}}{R_{ref}}\frac{255}{256}$$ (Full scale)

Pros:
- We can vary Vref in addition to Din

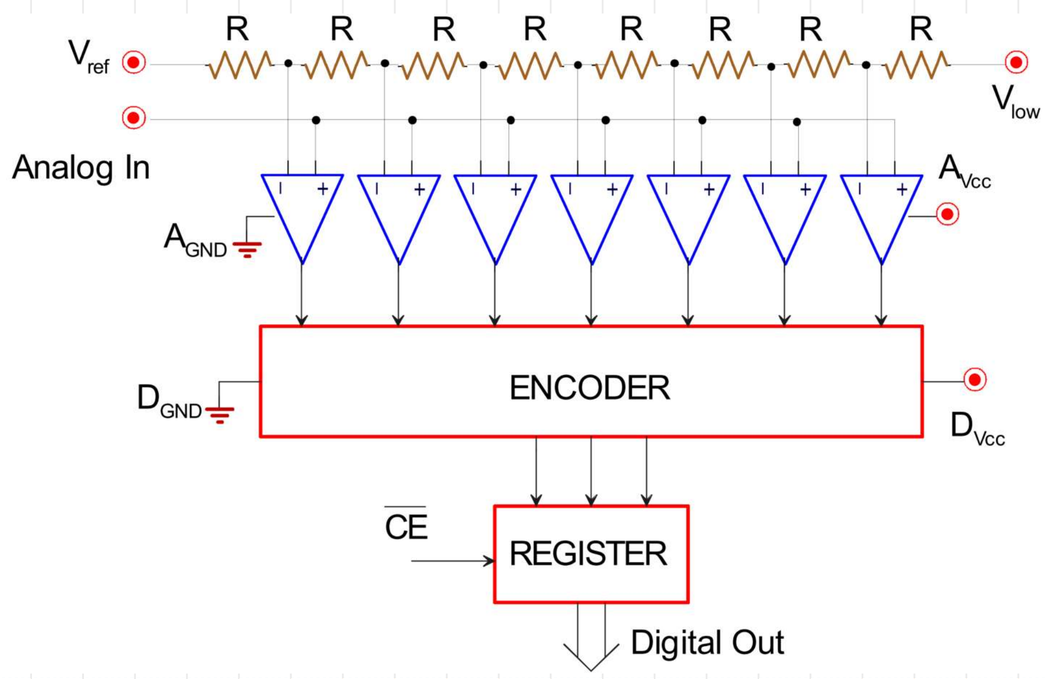
ADC summary



Formula: $Dout = \frac{Ain}{\frac{Vref}{2^n}}$

Std types:

• Flash ADC

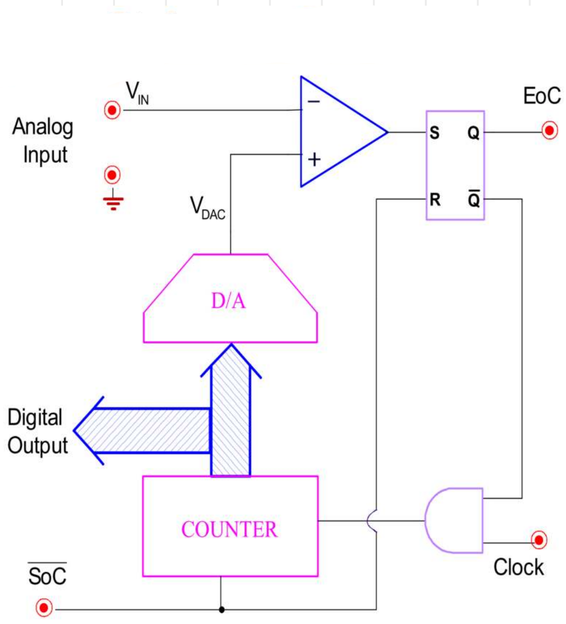


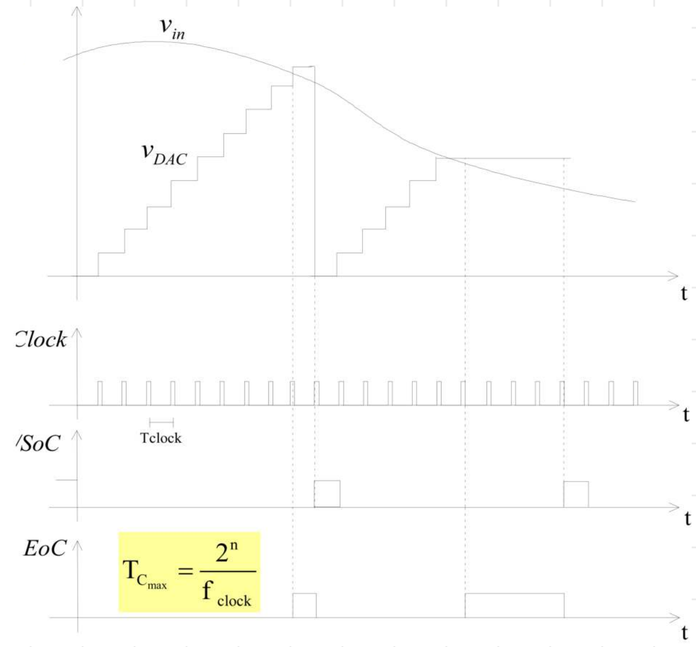
Components:
- 2^n resistors → to create 2^{n-1} quantization levels
- 2^n comparators → compares the q. levels with the input → H/L
- 1 encoder (thermometric code → binary code)
  - ↳ H/L → 0/1

Pros:
- very fast → parallel conversion
- simplicity

Cons:
- silicon area ↑ and power dissipation ↑ with n↑
- bias and leakage currents, parasitic capacitors
  - ↳ lead to non-lin. of the ADC converter
- offset lead to incorrect switching
  - ↳ missing codes, non-monotonicity of ADC

• Staircase ADC





Components:
- 1 Counter → subsequent adjustments via binary count
- 1 DAC → binary count $\xrightarrow{DAC}$ analog level to compare with Vin
- 1 comparator

Pros:
- precision depends on the DAC

Cons:
- Conversion time depend on Vin
  - ↳ not very fast
  - ↳ sampling comb not of const. (not regular sampl. steps due to time dep. on Vin)

Converts in hold phase ← you can put a S&H before the ADC (↳ regular)

• Tracking ADC

Components: 1 DAC, 1 counter, 1 comparator, 1 up/down logic

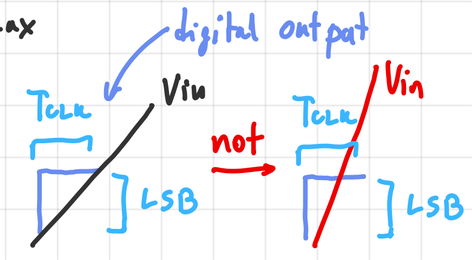
Components:
- 1 Counter → subsequent adjustments via binary count
- 1 DAC → binary count $\xrightarrow{DAC}$ analog level to compare with Vin
- 1 comparator
- 1 up/down logic → to make the counter go up/down and "track" Vin

Pros:
- Fast → correct sample at every CLK
- precision depends on DAC
- Oversampling → use just one bit = Up/Down to stay hooked on input signal

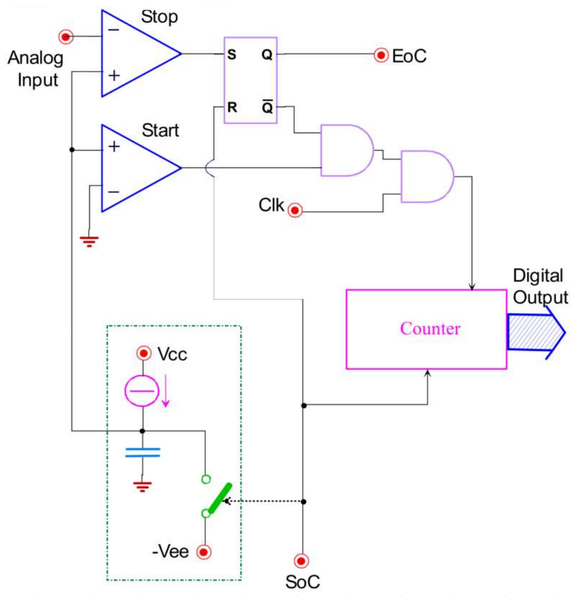
(also called Δ modulator)

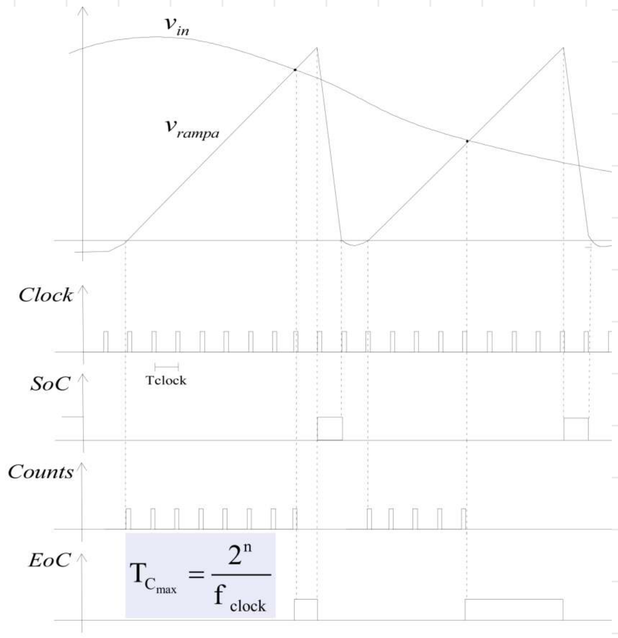
Cons:
- frequency of signal $\gg f_{max}$
  - ↳ $f_{clk} \geq 2^n \pi f_{max}$

for high slope $\left.\frac{dVin}{dt}\right|_{max} < \frac{LSB}{T_{CLK}}$



• Single-slope ADC





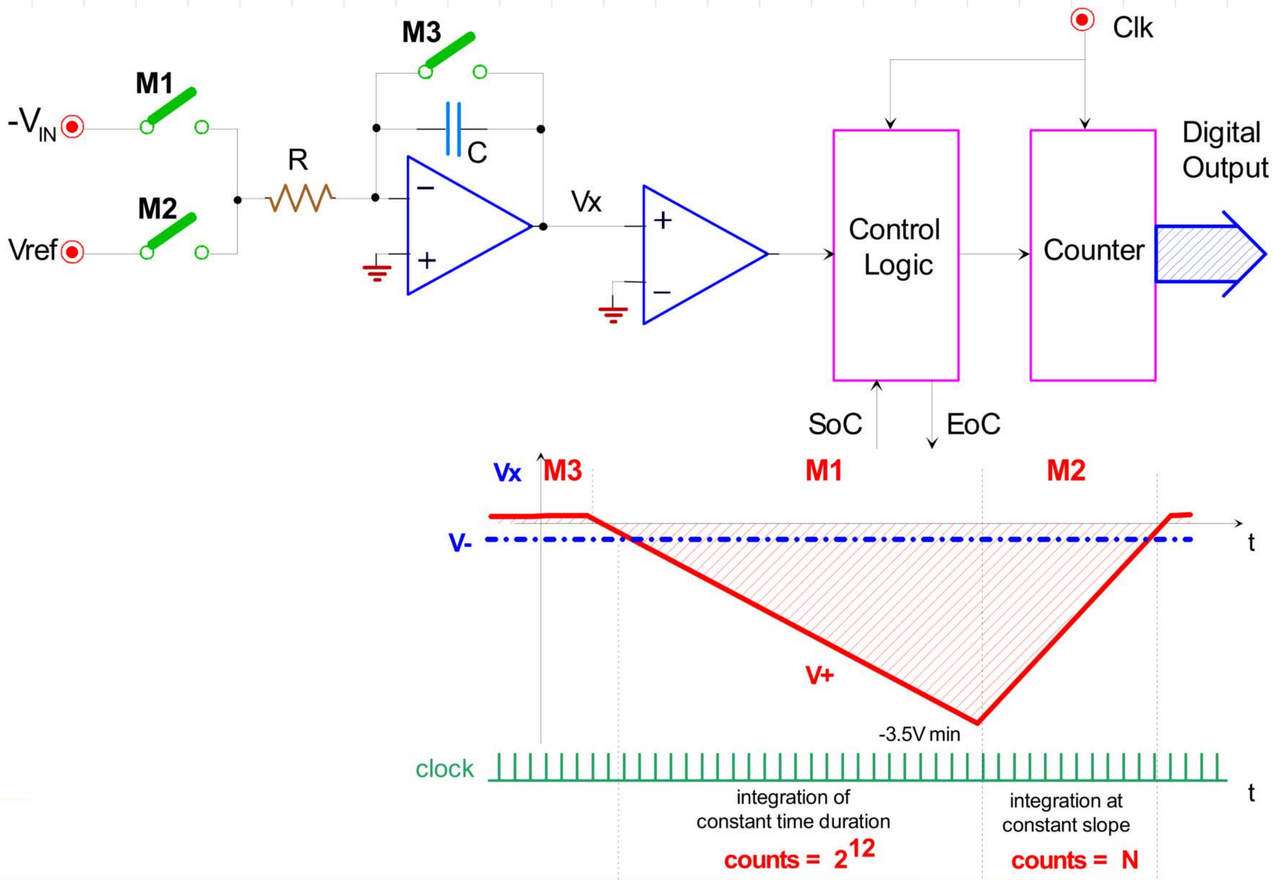
Components:
- const. current source → charges
- capacitor → linear charge → ramp
- comparator → ramp vs. Vin comparison
- counter → counts only after reaching Vin → digital output

Pros:
- precision dependent on $\frac{dV}{dt} = \frac{I}{C}$ → I source, C components
- many bit (n>16)

Cons:
- offset of comparator → make ramp start from slightly <0
- slow (like staircase problems)
- irregular sampling comb
- too sensitive to toll of C, I source, CLK period
  - ↳ low conversion accuracy

better to use double ramp.

• Dual-slope ADC

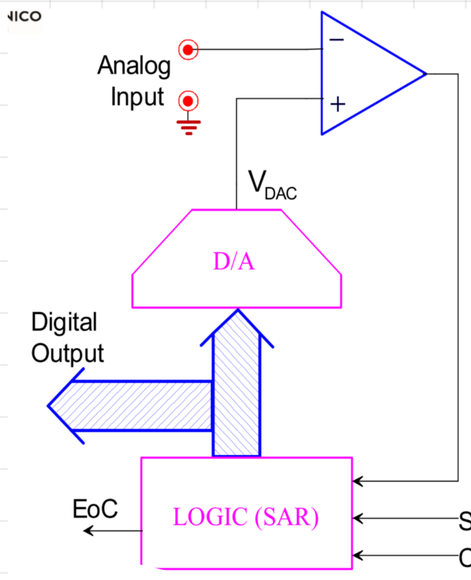


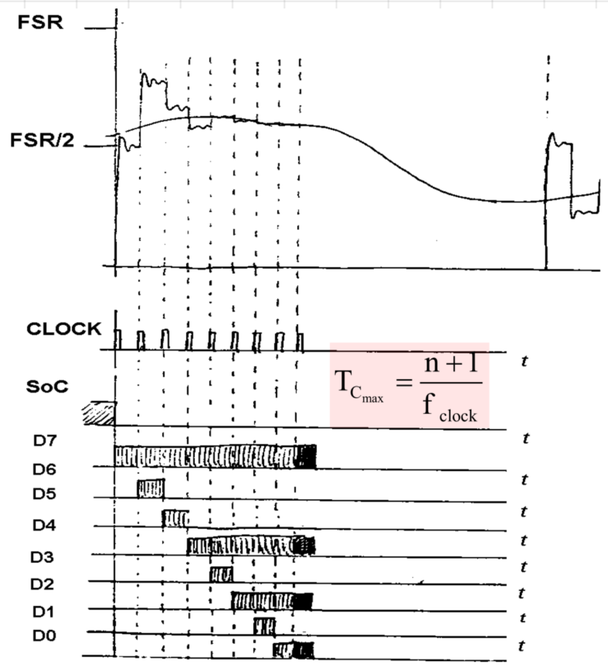
Components:
- integrating OpAmp → M1 → charge → to obtain a ramp α -Vin
  - discharge → M2 → to obtain a ramp from $\int$Vref (const.) (So const slope)
  - integration (for 2^n CLK pulses)
- counter → count CLK pulses for integrations phases
- control logic → switches control / SoC / EoC
- comparator → detect when the value stored across C is Ø again → $V_{ref} = V_{in}$

Pros:
- precision independent of R and C (their toll.)
  - ↳ both charge/discharge ramps with the same $\tau = RC$
- Disturbance rejection at freq = int. multiples of integration period
  - ↳ (NMR) (Normal Mode Rejection)

Cons:
- High conversion time → twice the one of Single-slope

• Successive approximation (SAR)



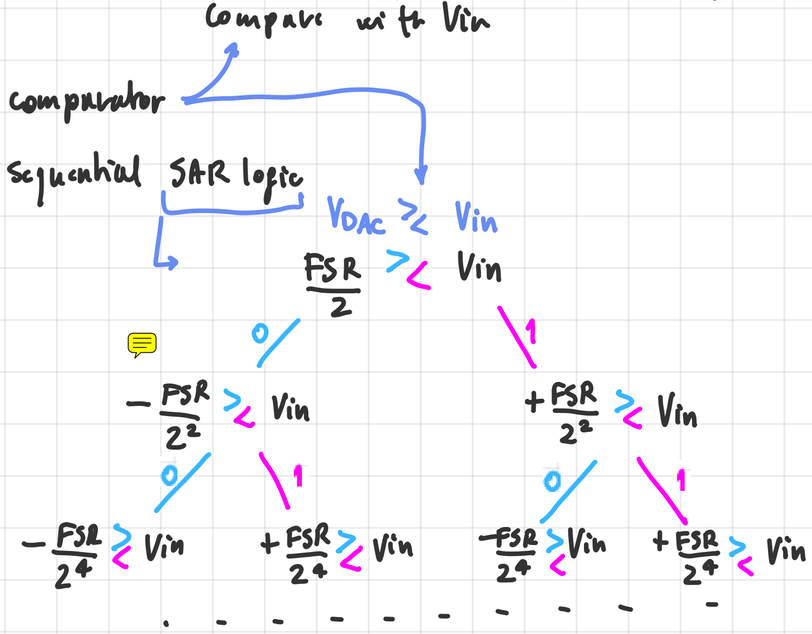


ponents: 1 DAC and 1 sequential SAR logic

ntages: precision depends on the DAC

many bit (n=8..14) and fast (T_C>10µs)

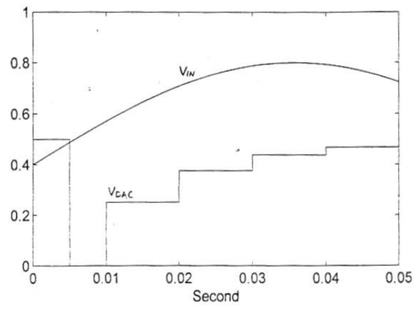
Components:
- 1 DAC → to convert digital levels to analog level to compare with Vin
- 1 comparator
- 1 sequential SAR logic



Pros:
- precision depends on DAC
- conversion requires only n+1 CLK pulses (instead of usual 2^n)

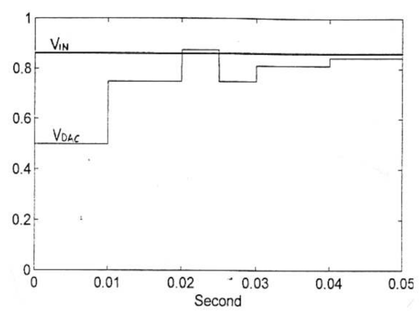
Cons:
- if too variable Vin → errors
  - ↑ put a S&H before ADC

Maximum input signal frequency:



With NO S&H at the input:

$$f_{in,max} \le \frac{f_{clock}}{2\pi \cdot 2^n \cdot (n+1)}$$

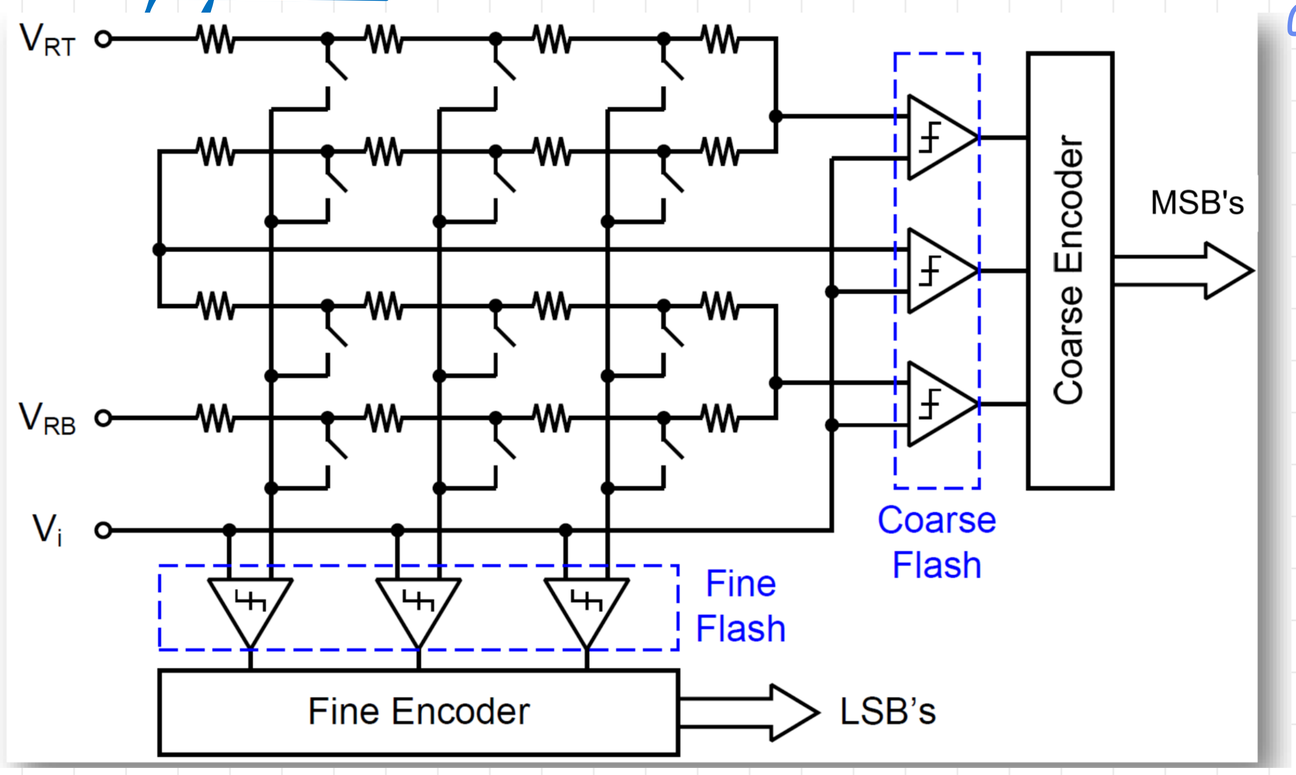


with S&H at the input:

$$f_{in,max} \le \frac{f_{sampling}}{2} = \frac{f_{clock}}{2 \cdot (n+1)}$$

Advanced OpAmps

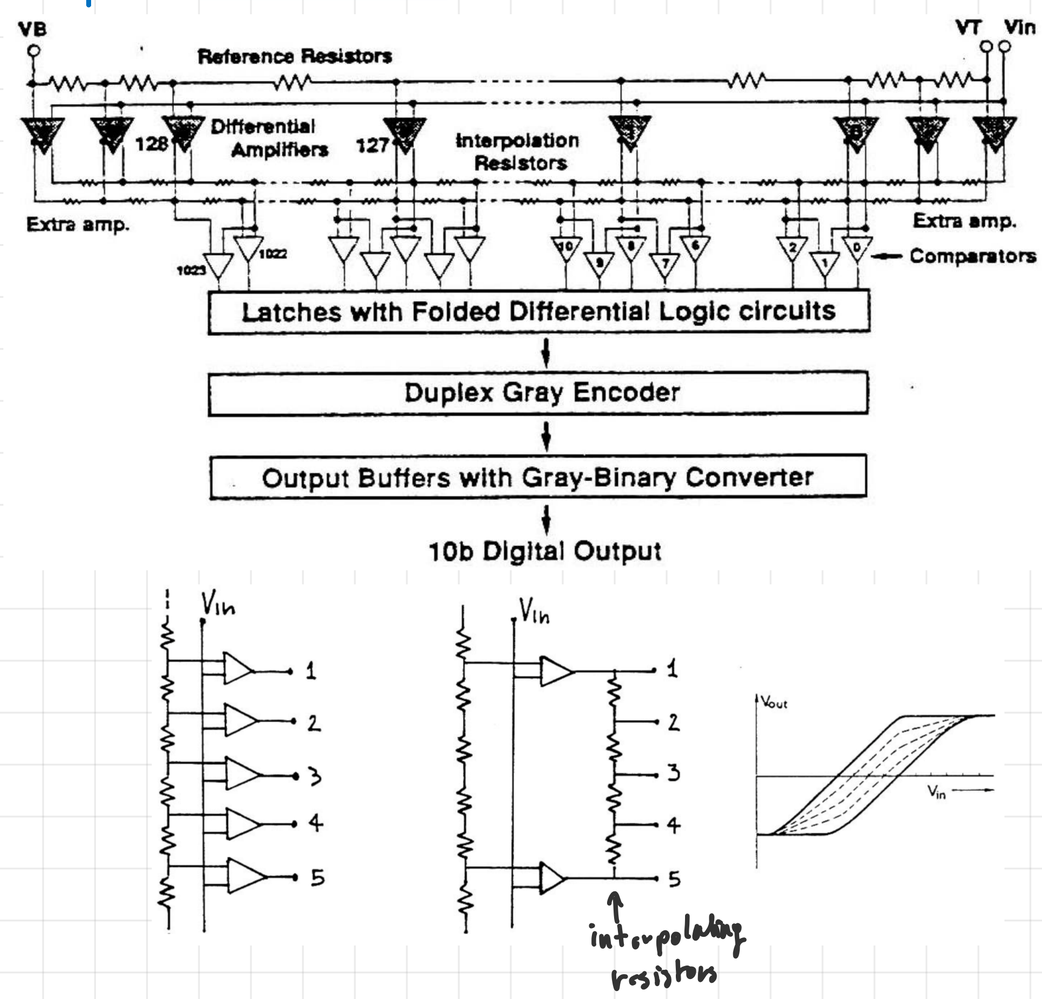
• Subranging ADC



Components:
- resistors → less for course conversion
  - → create quantization levels
  - → more for fine conv.
- comparators → compare levels with Vin
- encoders → (thermometric → binary)

Pros:
- less waste of resources
  - when far from Vin → COARSE: less resolution
  - when near Vin → small range → FINE: more resolution

• Interpolation Flash-ADC

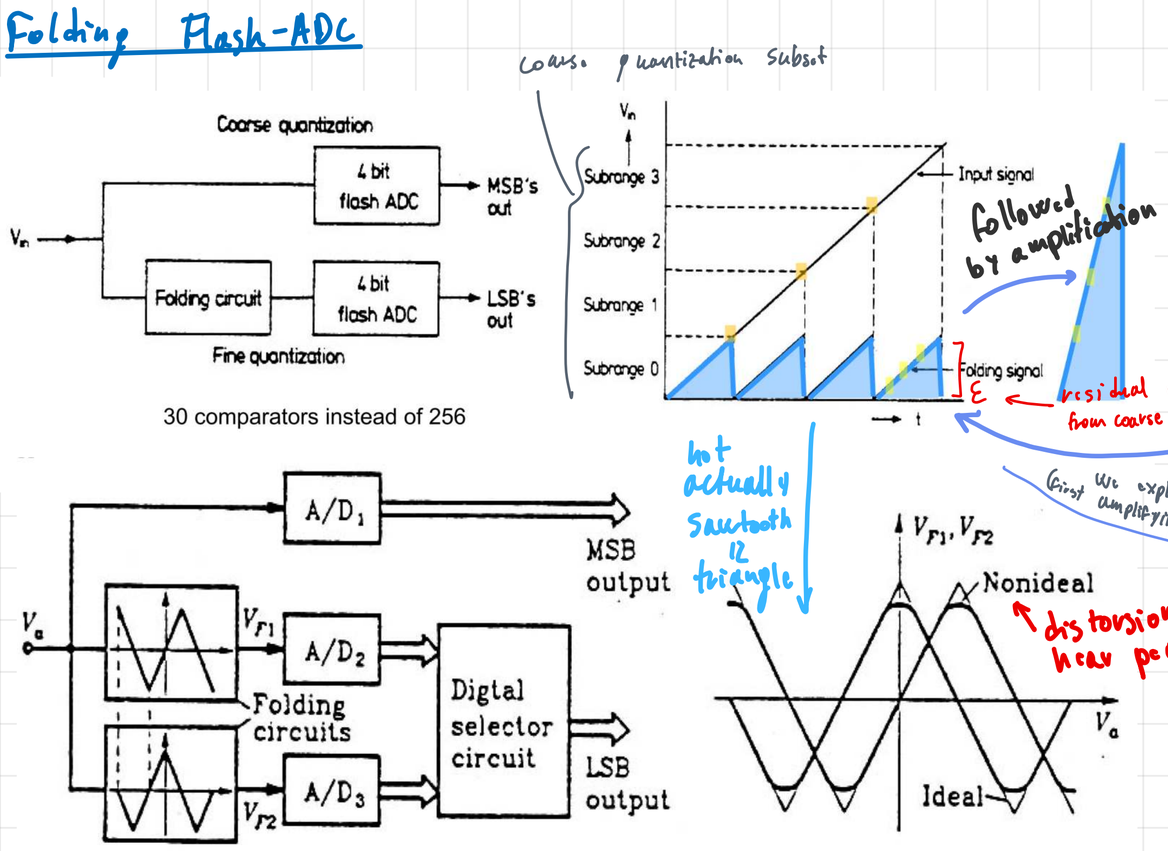


Components:
- resistors → reference
  - → interpolating → create levels from reference after comparison
- differential comparators → differential output

- latches with folded diff. logic circuit → sign of Vout
- Encoders

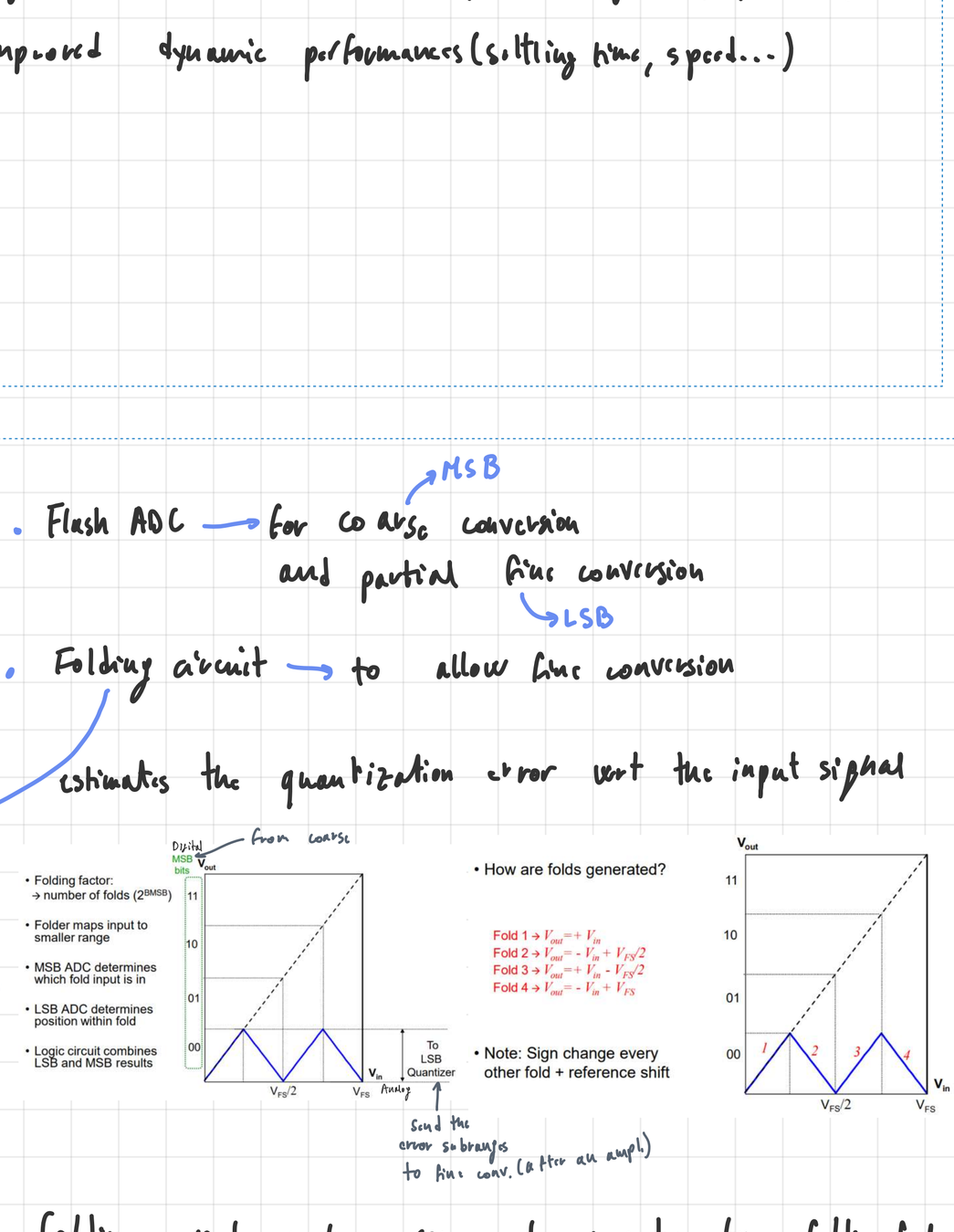
Pros:
- use less comparators without loosing levels
- huge reduction of silicon area, power dissipation, input stray C
- improved dynamic performances (settling time, speed...)

• Folding Flash-ADC



Components:
- Flash ADC → for coarse conversion (MSB) and partial fine conversion (LSB)
- Folding circuit → to allow fine conversion

estimates the quantization error vert the input signal

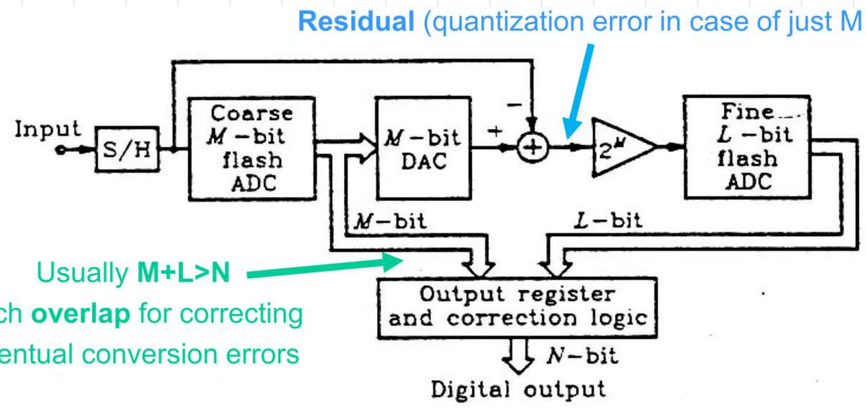


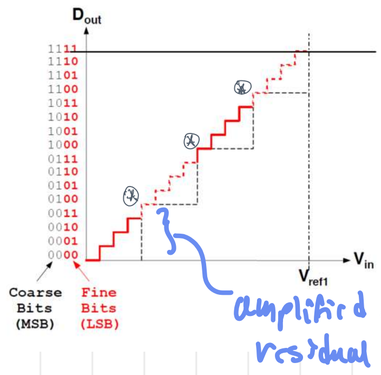
We explore the error ranges (first amplifying them) with fine conv.

Pros:
- Folding reduces the comparator number by a folding factor F (number of preamps stays the same)

Cons:
- folding signals can suffer from distorsion / non idealities on folding edges → use just zero-crossing

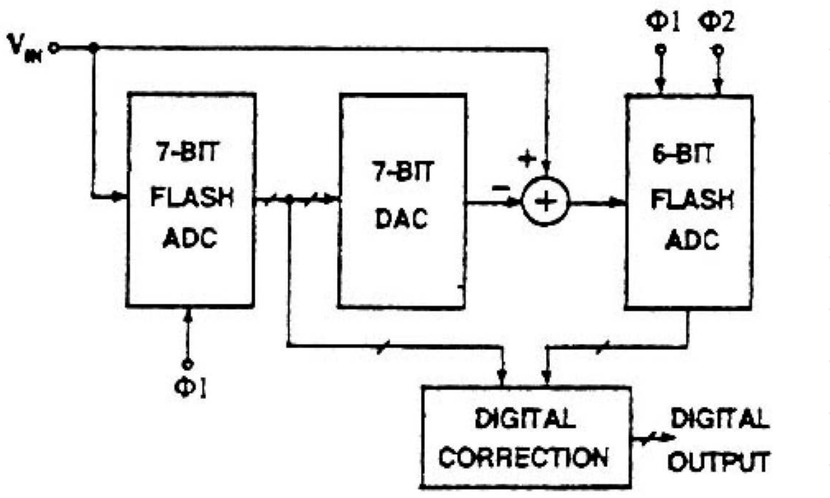
• Half-flash ADC





M coarse, L fine

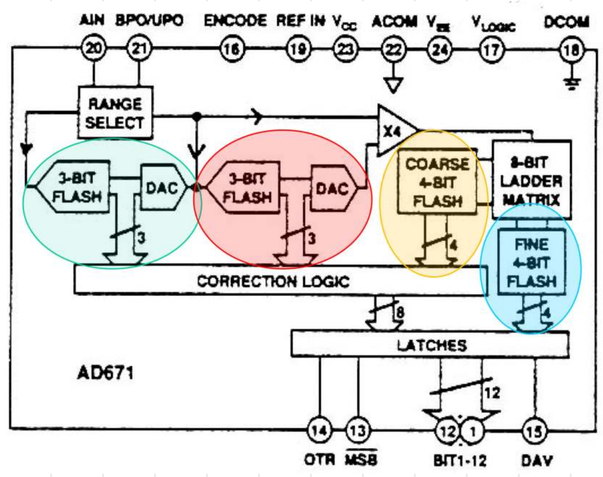
Components:
- low bit flash converters → for conversion stages
- DAC → convert first round of MSB to an A signal to feed then the Fine ADC (accuracy of at least N total ADC)
- Amplifiers → to amplify the residual coming from M bit coarse ADC quantization
  - we amplify the error resulting the ranges to quantize them with fine ADC
- sum and correction logic → for correction use M+L>N (Tot. bit)
  - overlapping bits correct any conversion edges → Nicola

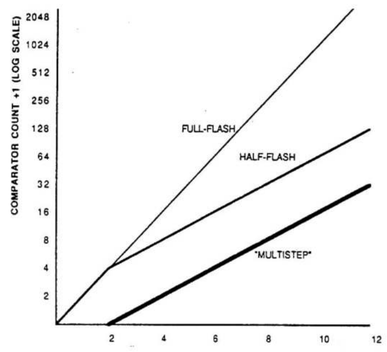


Pros:
- minimize area occupation and power consumption

Cons:
- slow conversion time

• Multistep ADC





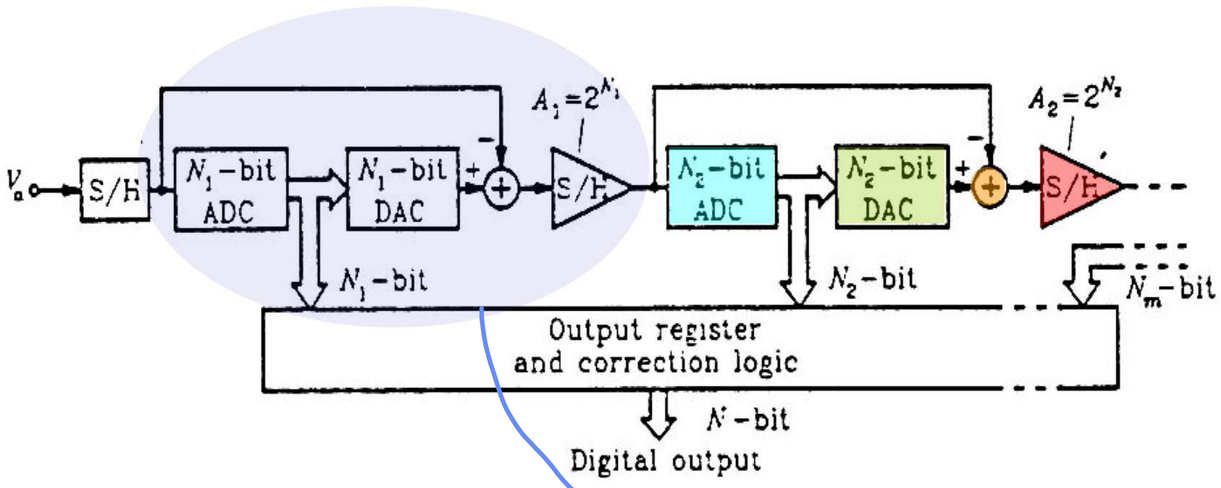
Components:
- same as previous flash solutions
  - but not only made of 2 stages
  - more stages in CASCADE

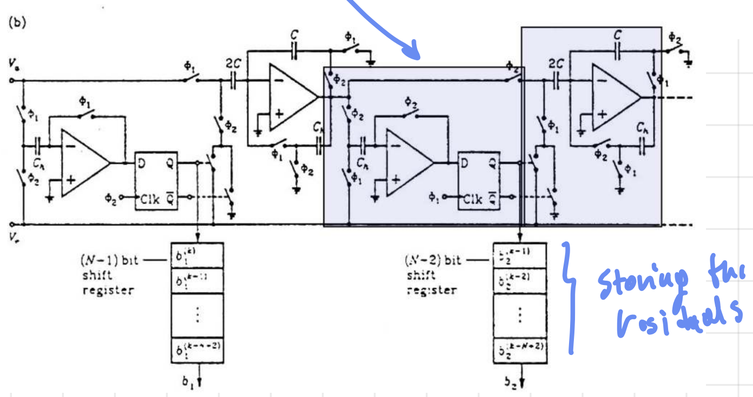
Pros:
- less comparators → (low area occupation)

Cons:
- conversion time ∝ # stages → slow!

better to use pipelined

• Pipelined ADC





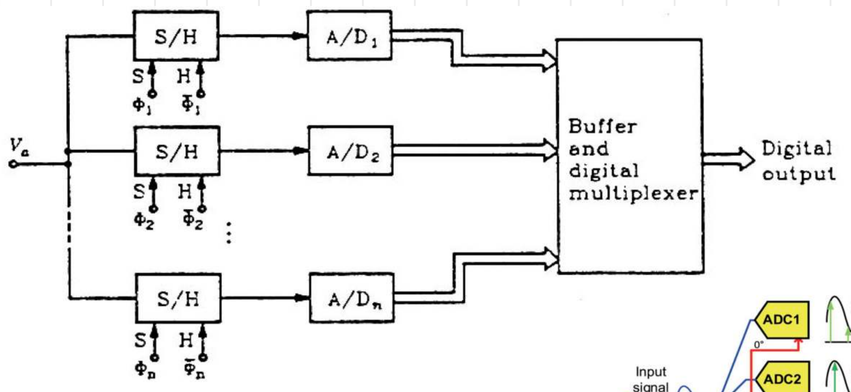
Components:
- same of half flash/multistop stages
  - + S&H → to put before every stage → we hold the residual value, so the stage can directly proceed with another conversion

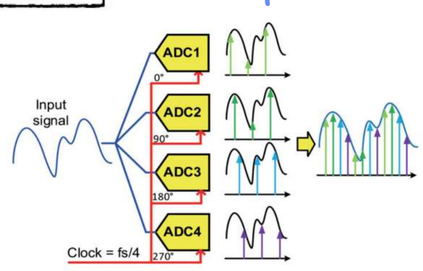
parallel-pipelined processing

Pros:
- fast conversion time
  - wrt Half-flash/multistep improves of a factor equal to # stages of pipeline
- low area occupation and power consumption

Cons:
- compromises bw speed and accuracy
  - m↑ conversion time↓ accuracy↓ (noise increases stage after stage)

• Time-interleaved ADC





channels operate in sequence

Components:
- ADCs → put in parallel
- S&H → put before every ADC

Pros:
- # stages faster wrt single channel
  - achieve conversion speed not possible with single converters

Cons:
- different channel behaviour, non regularity of sampling intervals
  - due to systematic errors bw channels
    - create spurious freq. components